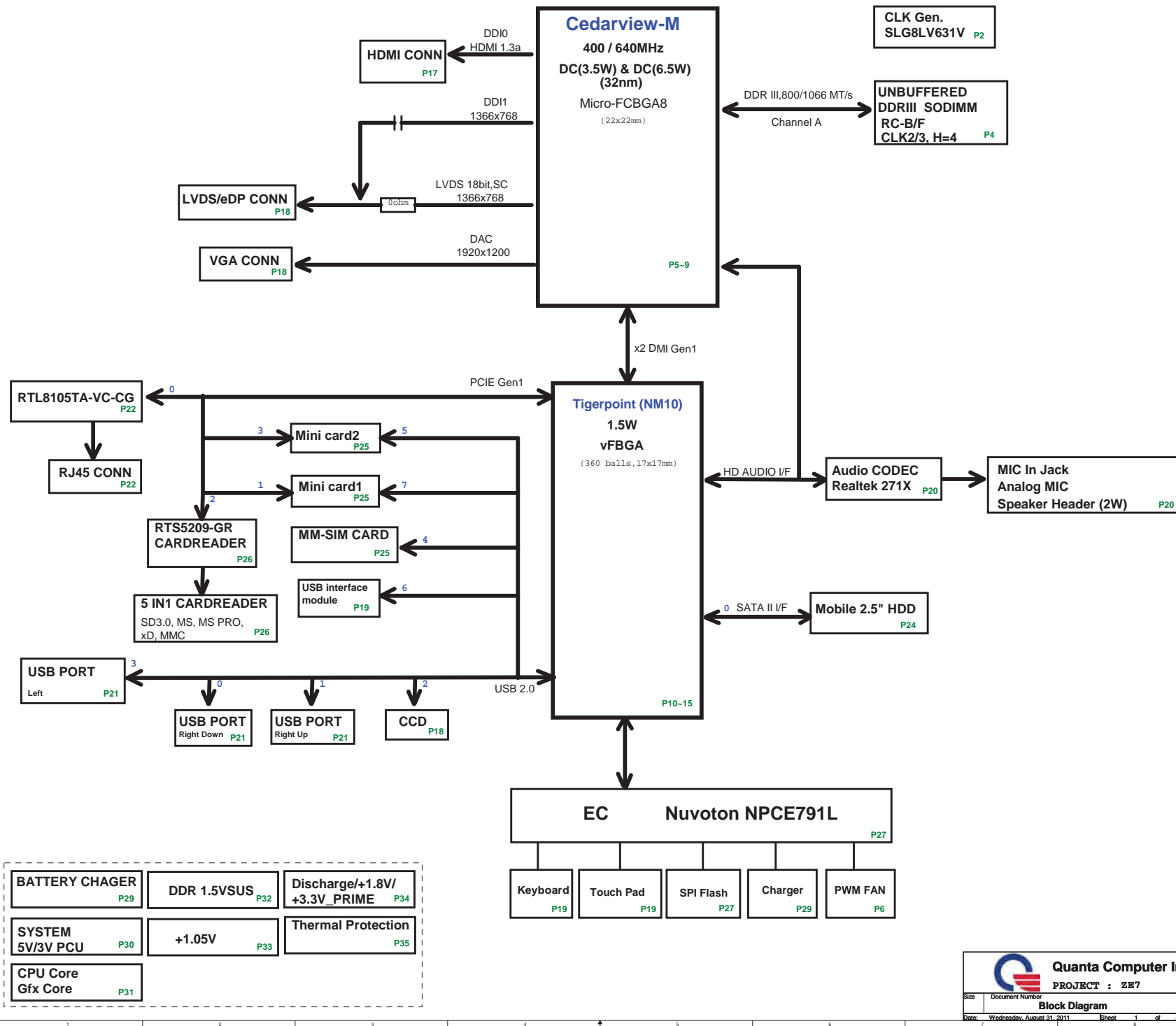
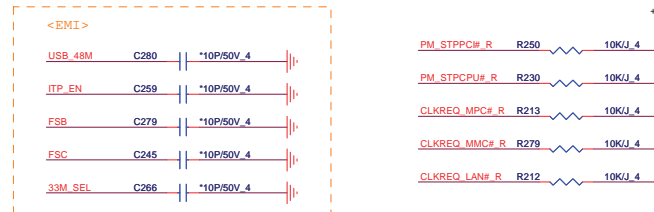
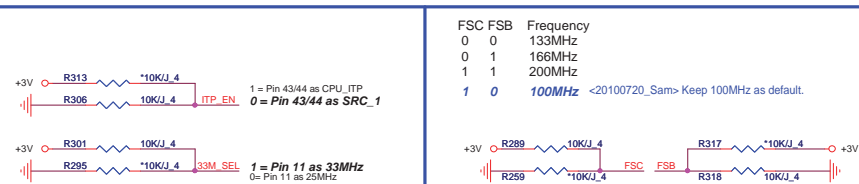
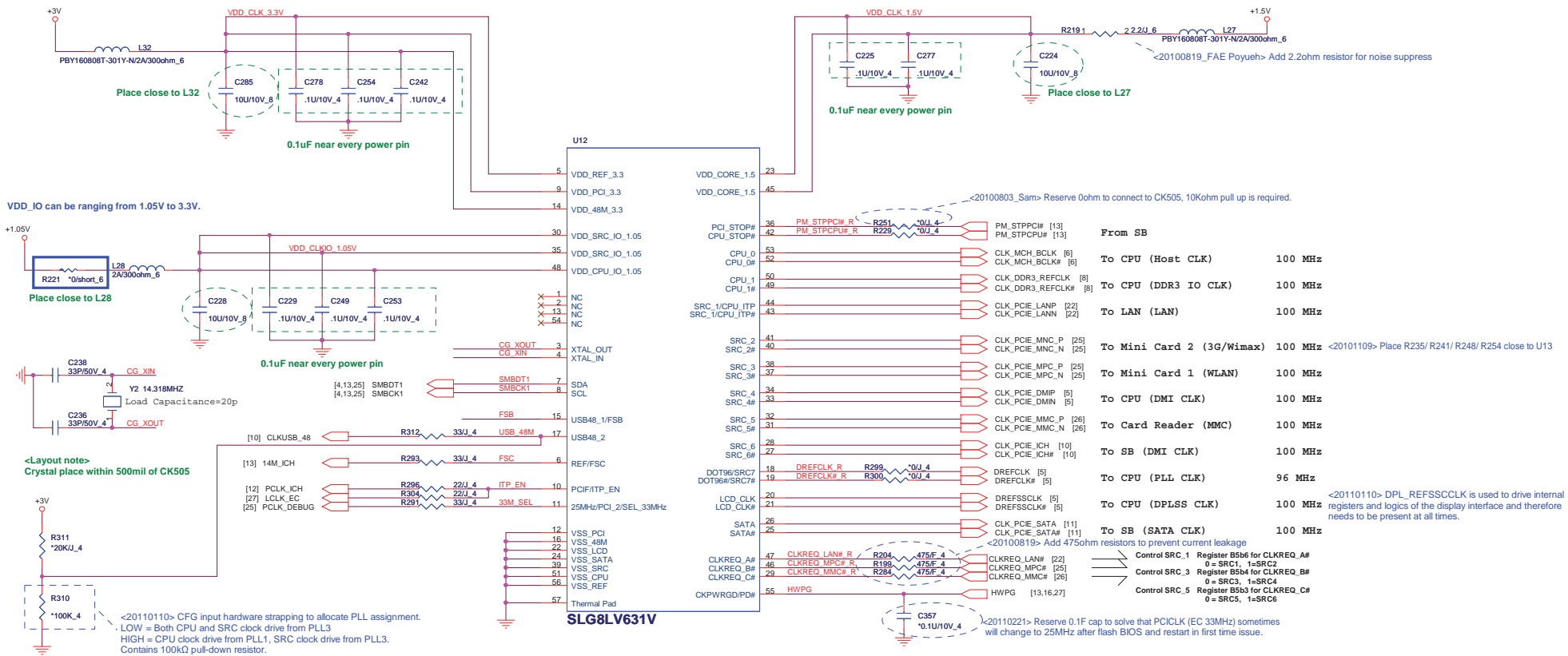


# ZE7 Block Diagram (Intel Cedar Trail-M Platform)

01

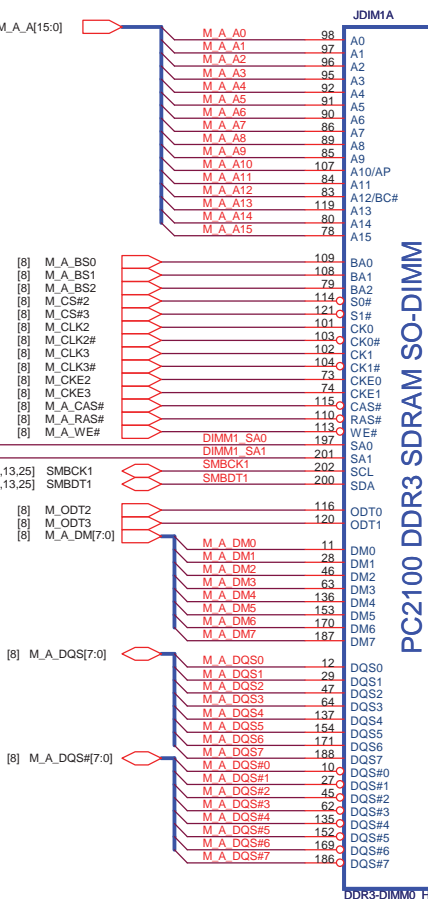
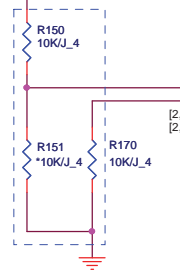




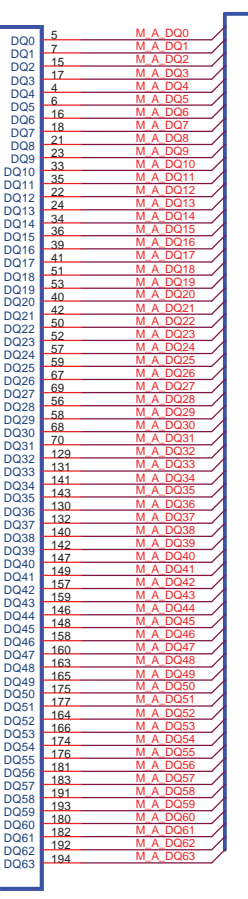


Populate rules: populate SODIMM1 first  
Strictly follow the mapping between clock/control signal groups and SODIMMs, as well as SMB address. Other configurations/mappings will not be supported by MRC

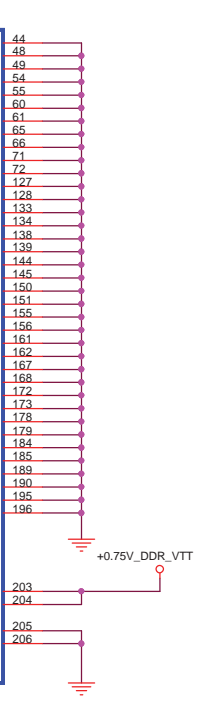
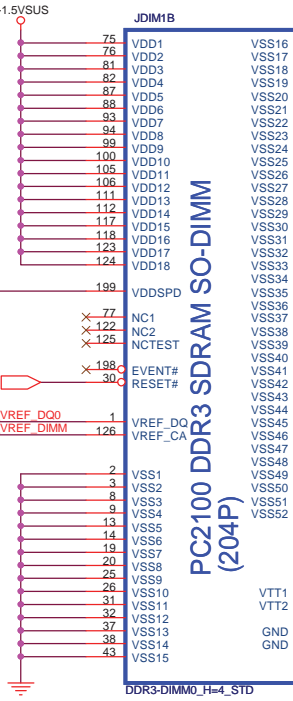
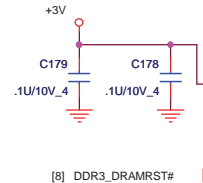
DESIGN NOTE:  
ADDRESS-(A2)H



PC2100 DDR3 SDRAM SO-DIMM (204P)

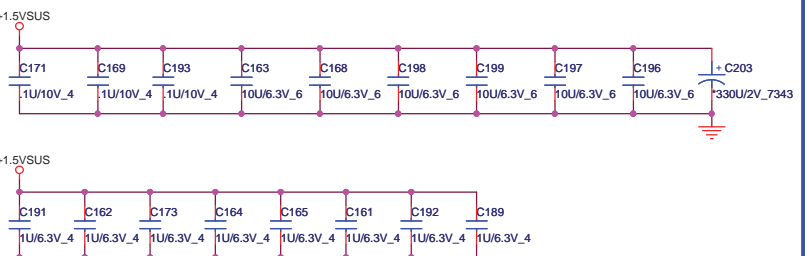


2.48A

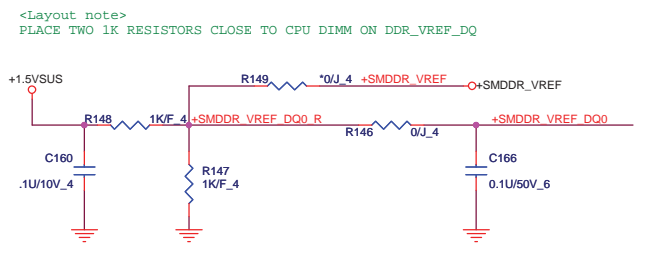
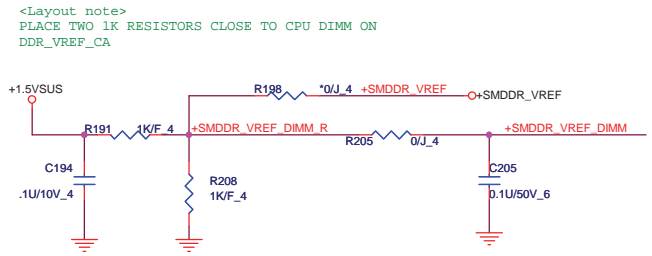
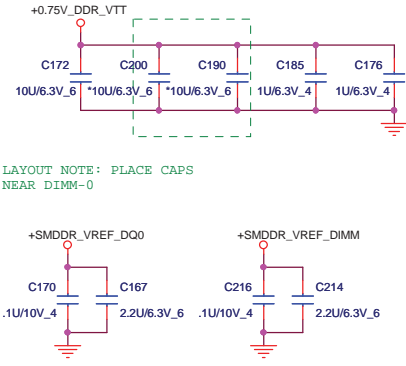


DDR3-DIMM0\_H=4\_STD

Place these Caps near DIMM0



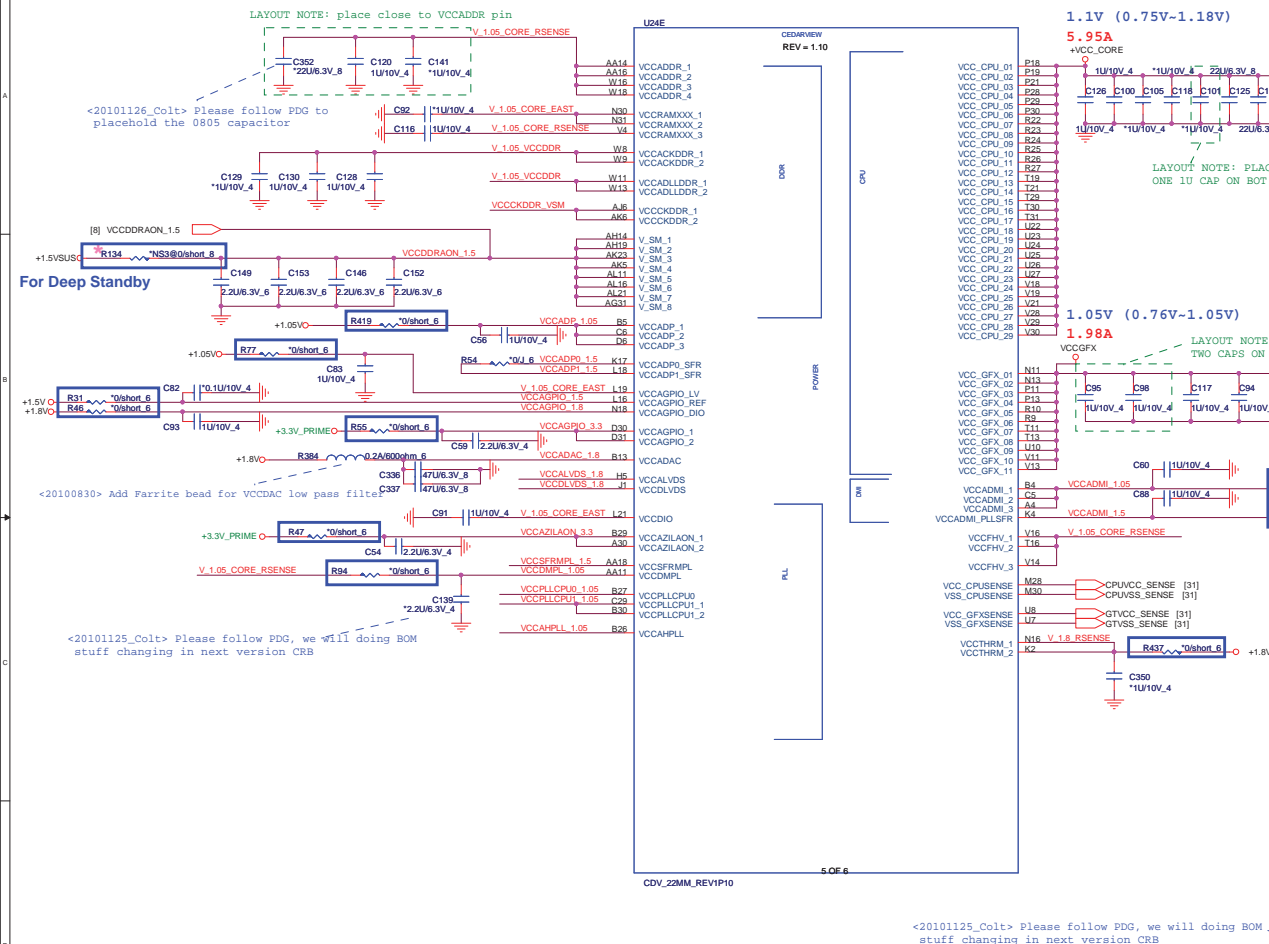
<20100827> Add by DG request





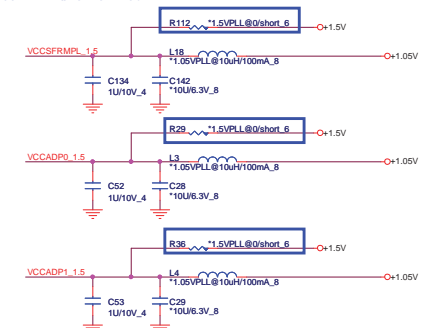


### Cedar View (CPU)



### Cedar View PLL Power

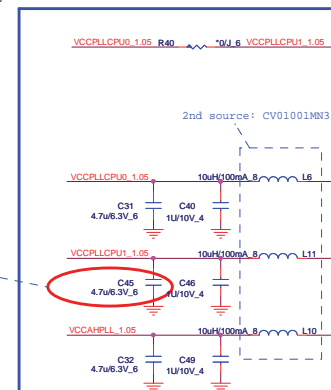
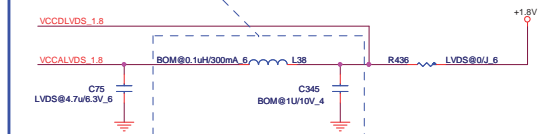
Default stuff 1.5VPLL, Intel verify whether 1.05VPLL is ok or not



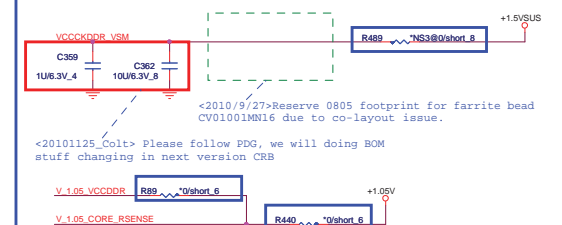
## Cedar View LVDS Power

## BOM structure

```
w/LVDS: stuff R436/ C345/ L38/ C75
w/EDP: unstuff R436/ C75
      change L38/ C345 to 0ohm
```



LAYOUT NOTE: OVERLAP RESISTOR AND INDUCTOR



**Quanta Computer Inc.**

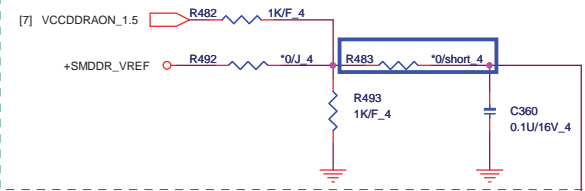
PROJECT : ZE7

|       |                            |               |
|-------|----------------------------|---------------|
| Size  | Document Number            | Rev           |
|       | <b>CedarView Power</b>     | C3C           |
| Date: | Wednesday, August 31, 2011 | Sheet 7 of 42 |

# Cedar View (CPU)

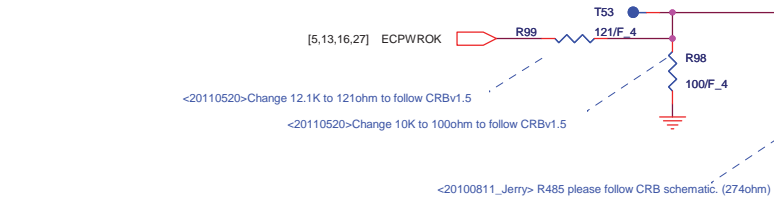
08

<Layout note>  
PLACE RESISTORS AND CAP CLOSE TO CPU DDR\_VREF PIN

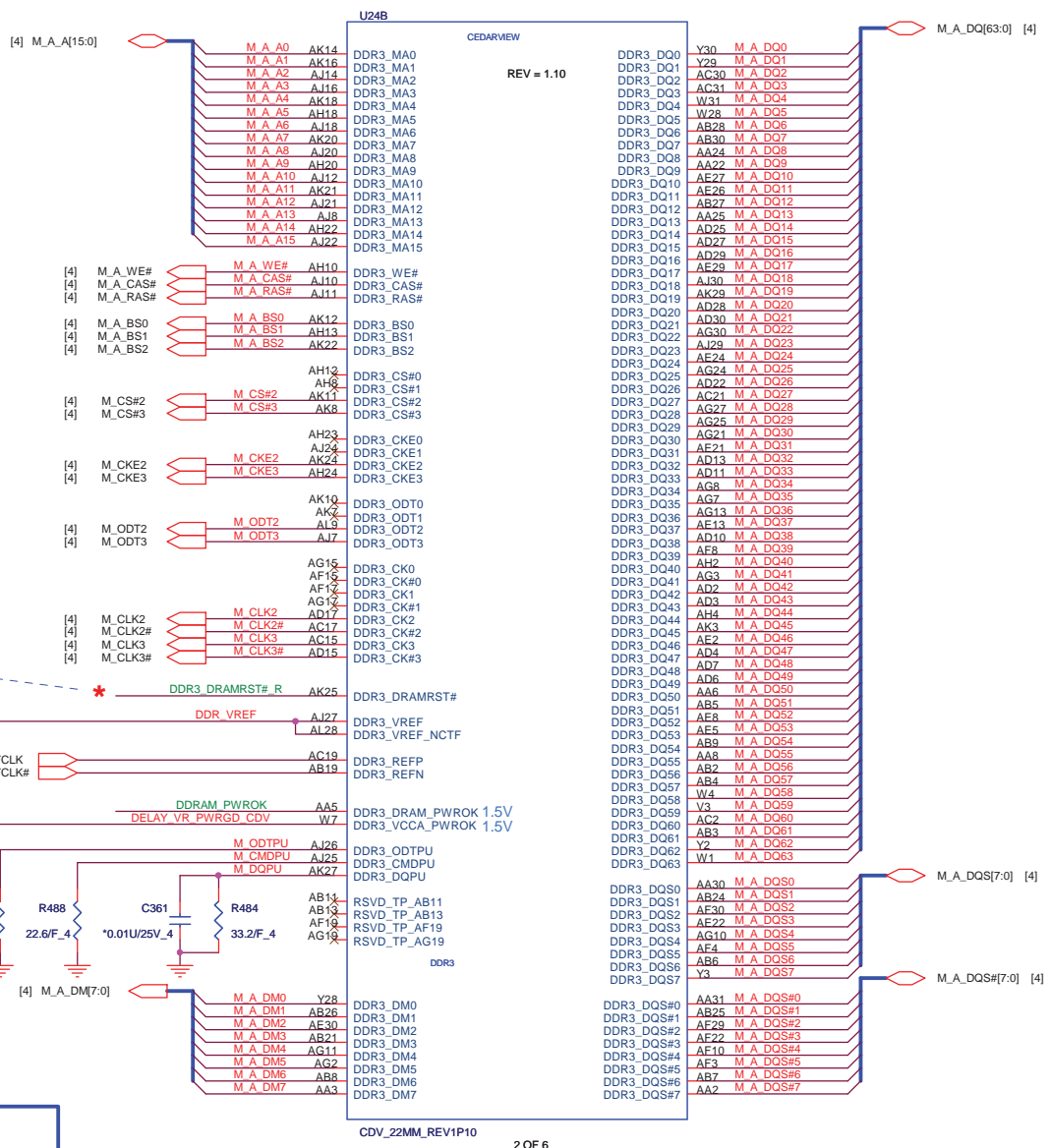
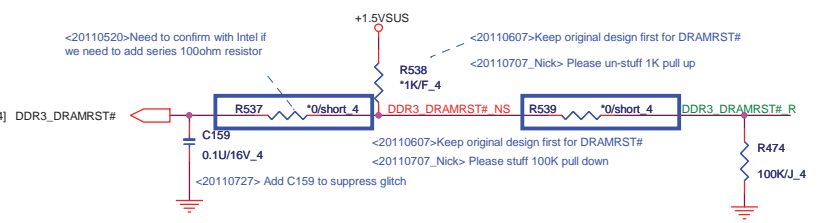


<20100810\_Jerry> Please refer to Cedar Trail CPET HW section(#454349), it is to implement Deep Standby. And please waiting the whitepaper for implementation detail.

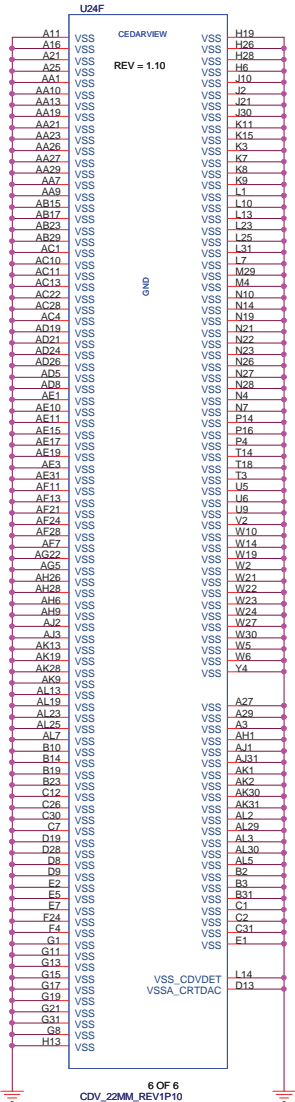
<20100817\_Jerry> DELAY\_VR\_PWRGOOD on CDV should be connected to the XDP\_PWRGOOD because the SV folks expressed a preference on using PWRGOOD over PWRGOOD for CDV. This has changed from PNV to CDV.



## DRAM Reset (CPU)

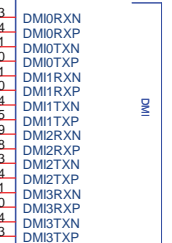
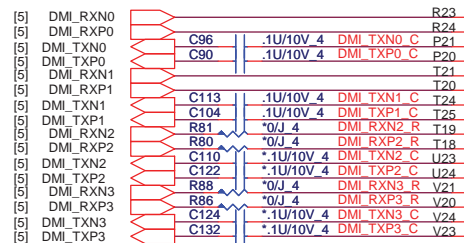






## Tiger Point (CLG)

U22B TGP



SYSTEM (Right Down)  
SYSTEM (Right Up)  
CCD  
SYSTEM (Left/ USB Charger)  
SIM  
3G  
BT  
WLAN

USB

PCI-E

Tiger Point

2

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

OC0# GPIO26 D4 USBOC#R 1 R435 \*0/short 4

OC1# GPIO27 C5 USBOC#R 1 R433 8.2K/J 4

OC2# GPIO28 D3 USBOC#R 1 R429 8.2K/J 4

OC3# GPIO29 D2 USBOC#L 1 R432 1K/F 4

OC4# GPIO30 E8 USBOC#

OC5# GPIO31 C2 USBOC#

OC6# GPIO32 C3 USBOC#

OC7# GPIO33

USBRBIAS G2 USBRBIAS R438 22.6/F 4

USBRBIAS G3

CLK48 F4 CLKUSB\_48 CLKUSB\_48 [2]

EMI

R66 \*10/F\_4

C81 \*10P/50V\_4

+1.5V R425 24.9/F 4 DMI\_COMP H24 J22

CLK\_PCIE\_ICH# W23

CLK\_PCIE\_ICH W24

DMI\_ZCOMP DMI\_IRCOMP

DMI\_CLKN DMI\_CLKP

2

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

LAN

WLAN

Card Reader

Media Processor

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5

USBOC#R 1 R435 \*0/short 4

USBOC#L 1 R427 \*0/short 4

USBOC#R 1 R433 8.2K/J 4

USBOC#L 1 R429 8.2K/J 4

USBOC# R432 1K/F 4

CRB ties unused OC pins together with 1k ohm

+3V\_S5



Quanta Computer Inc.

PROJECT : ZE7

| Size | Document Number          | Rev |
|------|--------------------------|-----|
|      | Tiger Point DMI/PCIE/USB | C3C |


Date: Wednesday, August 31, 2011 Sheet 10 of 42

1. CPUSLP# is supported only on nettop platforms.

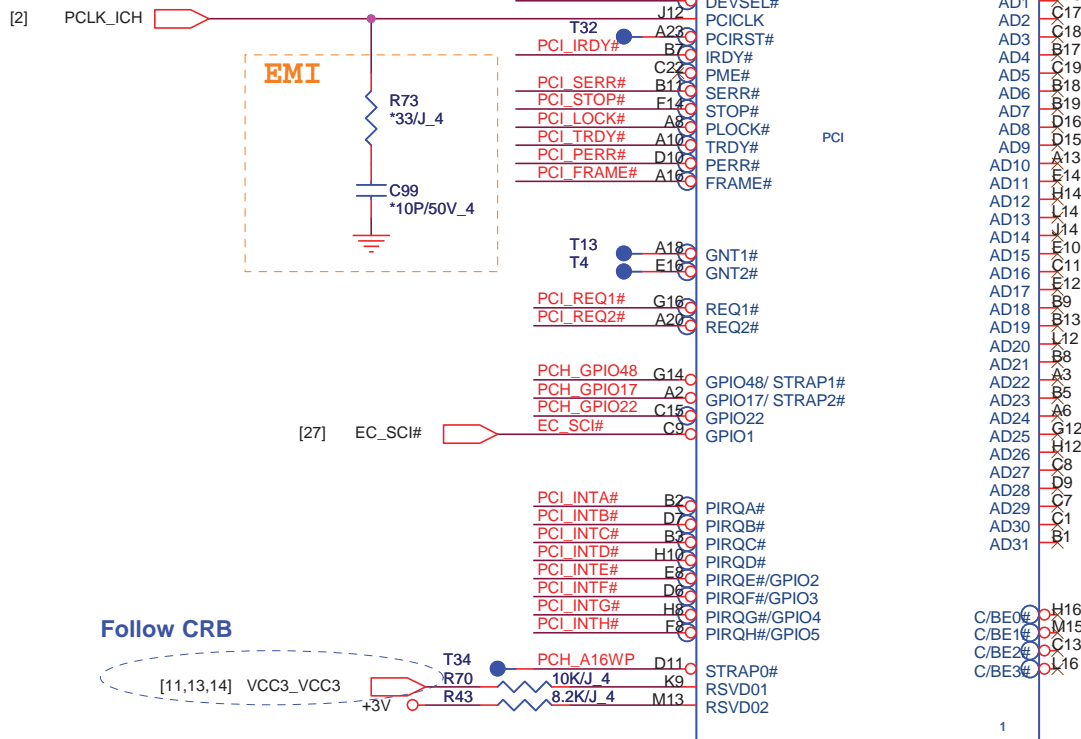


<20110607\_C-stage> Stuff 1K to follow CRB V1.5



|   |                            |                |
|---|----------------------------|----------------|
|  <div style="display: inline-block; vertical-align: middle;"> <b>Quanta Computer Inc.</b><br/> <b>PROJECT : ZE7</b> </div> |                            | Rev            |
| Size  | Document Number            | C30            |
| <b>Tiger Point Sata/Host</b>  |                            |                |
| Date:   | Wednesday, August 31, 2011 | Sheet 11 of 42 |

## PCI CLK 33M-Hz



<20090601(A1A)\_Checklist Rev0.7>  
Strap1#/strap2#: signals have weak internal pull-ups

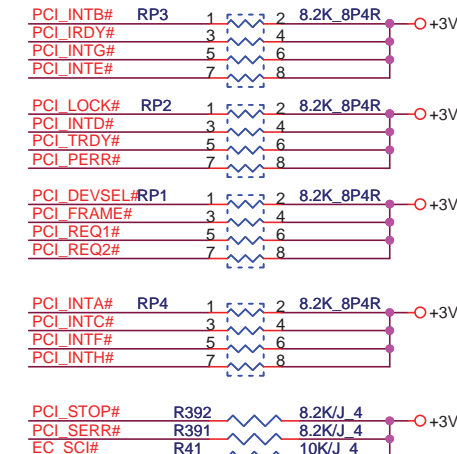
## ICH Boot BIOS select

| PCH_GPIO17 (INT PU) | PCH_GPIO48 (INT PU) | Boot BIOS Location  |
|---------------------|---------------------|---------------------|
| 0                   | 1                   | SPI                 |
| 1                   | 0                   | PCI                 |
| 1                   | 1                   | LPC (CURRENTLY USE) |

## A16 SWAP Override strap

| PCH_A16WP (INT PU) | Low = A16 swap override enabled<br>High = Default |
|--------------------|---|
|--------------------|---|

| PCI_GNT#2 | Internal PU<br>Should not be PD |
|-----------|---------------------------------|
|-----------|---------------------------------|



<20101104> Reserve R389(PCH\_GPIO22 PD) for 27MHz or 96MHz choosing, need vBIOS support  
Pull up --> for 27MHz  
Pull down --> for 96MHz

| IRQ   | Description  |
|-------|--|
| PIRQA | USB UHCI Controller #1, #4                           |
| PIRQB | AC'97 Codec; option for SMBUS                        |
| PIRQC | USB UH Controller #3; SATA/IDE Native Mode           |
| PIRQD | USB UHCI Controller #2                               |
| PIRQE | Internal LAN; Option for SCI, TCO, HPET#0,1,2        |
| PIRQF | Option for SCI, TCO, HPET#0,1,2                      |
| PIRQG | Option for SCI, TCO, HPET#0,1,2                      |
| PIRQH | USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2 |

**Quanta Computer Inc.**  
**PROJECT : ZE7**

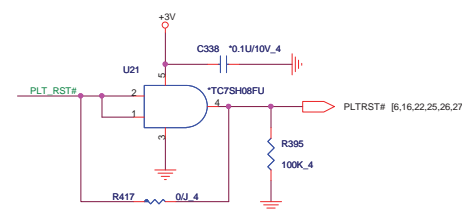
|      |                 |     |
|------|-----------------|-----|
| Size | Document Number | Rev |
|      |                 | C3C |

**TigerPoint PCI**

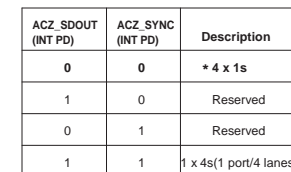
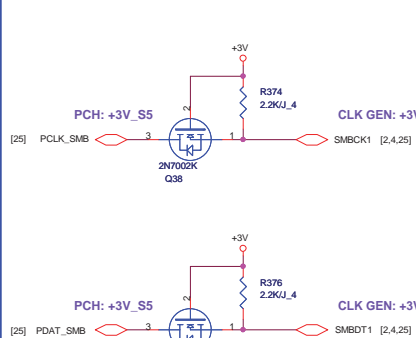
Date: Wednesday, August 31, 2011 Sheet 12 of 42




## Platform Reset (CLG)



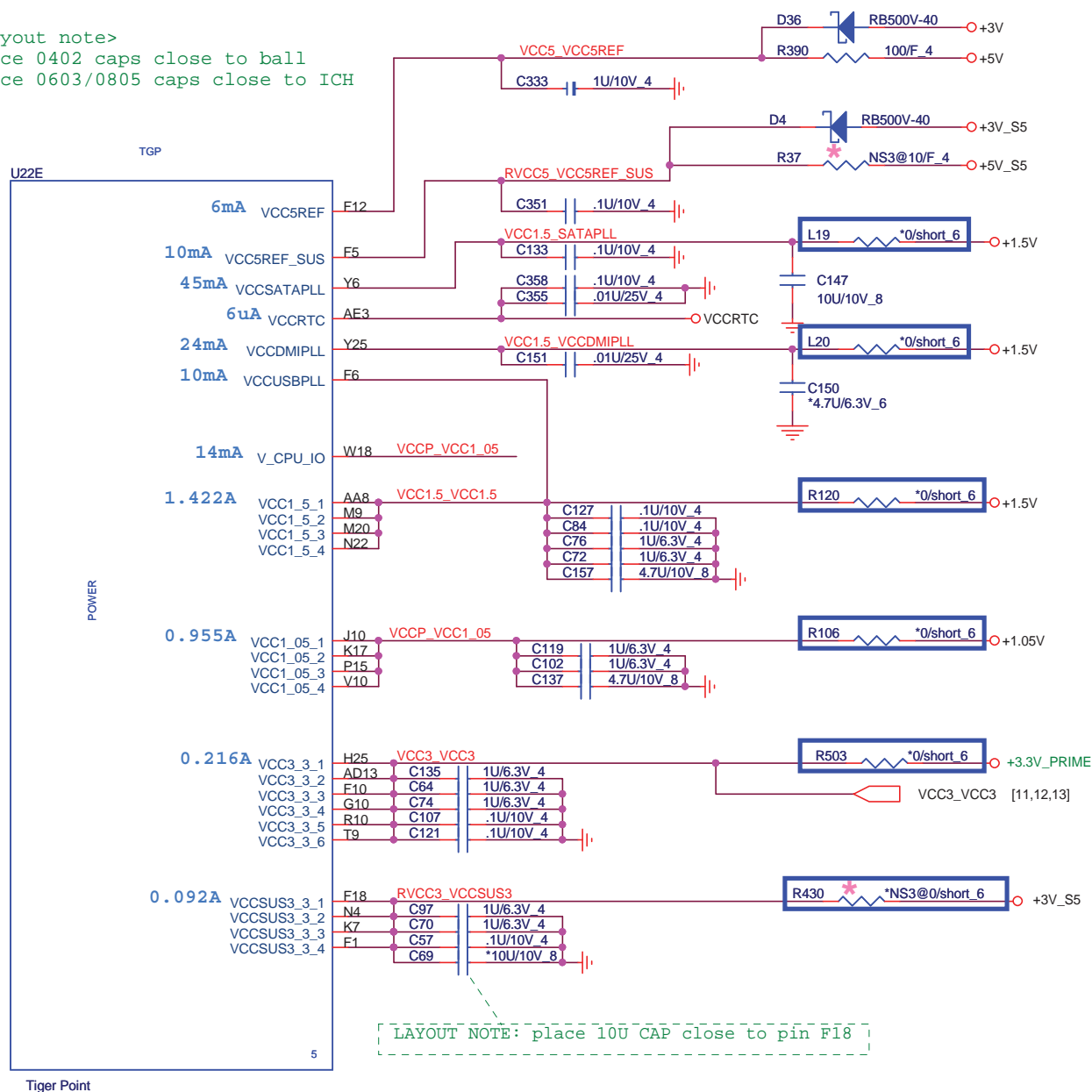
### Mother Board ID (CLG)



|   |                            |                |
|---|----------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZE7</b> |                            |                |
| Size  | Document Number            | Rev            |
|   | <b>TPT ACZ/GPIO/RTC</b>    | <b>C3</b>      |
| Date:   | Wednesday, August 31, 2011 | Sheet 13 of 42 |

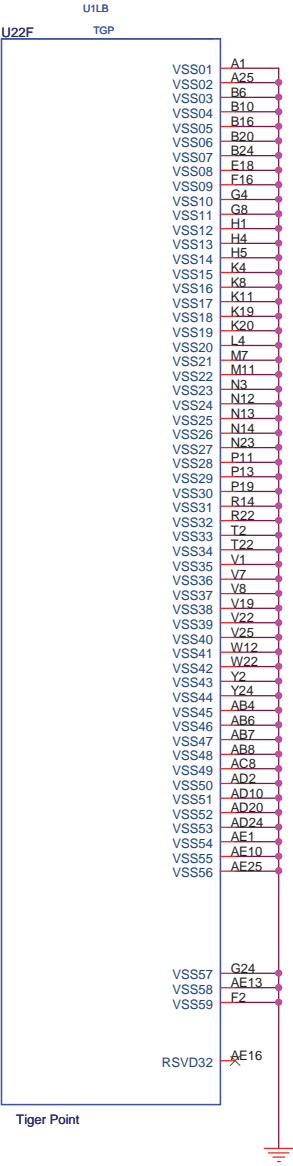
<Layout note>

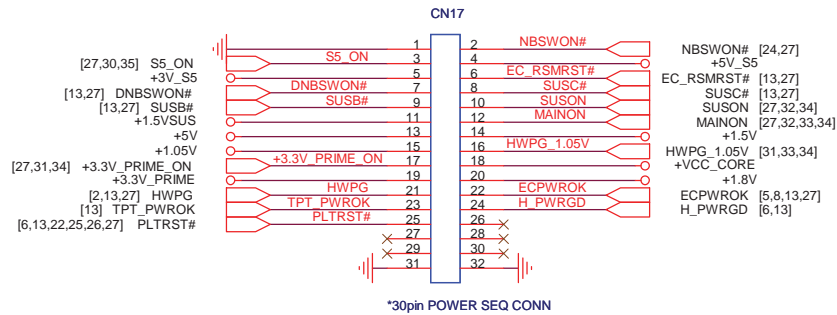
Place 0402 caps close to ball  
Place 0603/0805 caps close to ICH




Quanta Computer Inc.

PROJECT : ZE7





|    |          |    |             |    |           |
|----|----------|----|-------------|----|-----------|
| 1  | GND      | 11 | +1.5VSUS    | 21 | HWPG      |
| 2  | NBSWON#  | 12 | MAINON      | 22 | ECPIWROK  |
| 3  | S5_ON    | 13 | +5V         | 23 | TPT_PWROK |
| 4  | +5V_S5   | 14 | +1.5V       | 24 | H_PWROK   |
| 5  | +3V_S5   | 15 | +1.05V      | 25 | PLTRST#   |
| 6  | RSMRST#  | 16 | HWPG_1.05V  | 26 | RESERVE   |
| 7  | DNBSWON# | 17 | VRON        | 27 | RESERVE   |
| 8  | SUSC#    | 18 | +VCC_CORE   | 28 | RESERVE   |
| 9  | SUSB#    | 19 | +3.3V_PRIME | 29 | RESERVE   |
| 10 | SUSON    | 20 | +1.8V       | 30 | RESERVE   |



Quanta Computer Inc.

PROJECT : ZE7

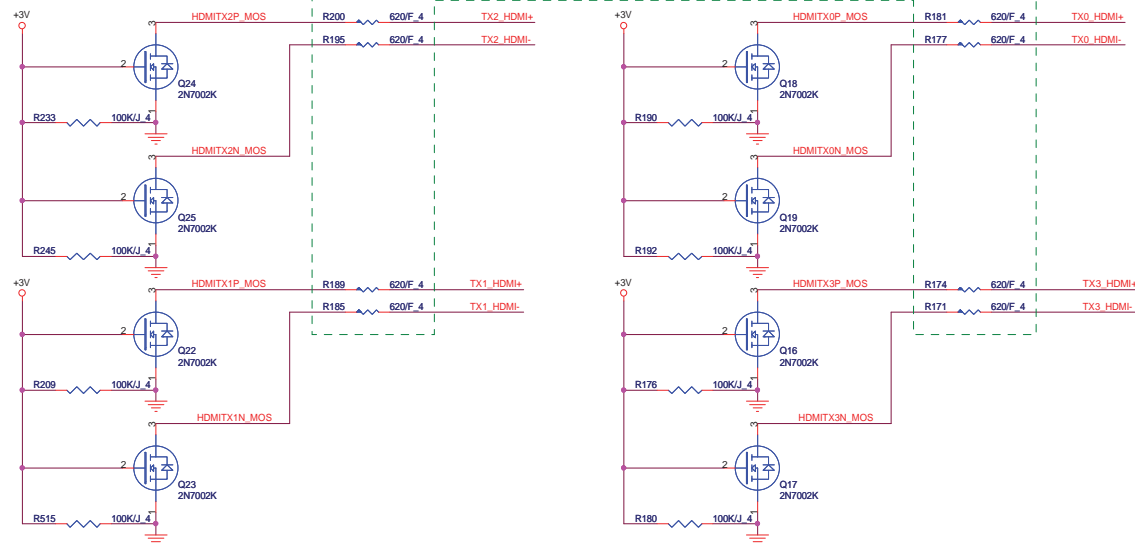
|       |                            |                |
|-------|----------------------------|----------------|
| Size  | Document Number            | Rev            |
|       | Cedarview XDP              | C3C            |
| Date: | Wednesday, August 31, 2011 | Sheet 16 of 42 |



## HDMI (HDM)

Level Shifter motherboard topology for max data rate of 1.65Gb/s

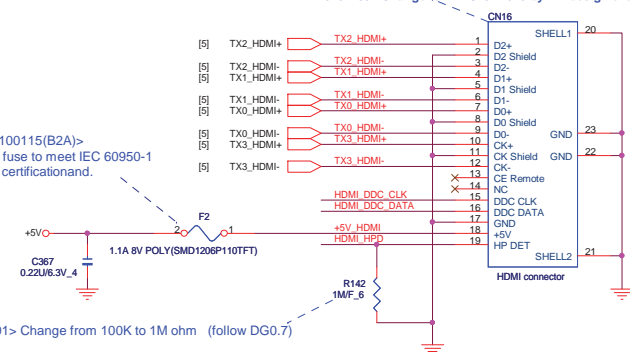
Close to HDMI connector



<20100115(B2A)>  
Add fuse to meet IEC 60950-1  
2nd certification.

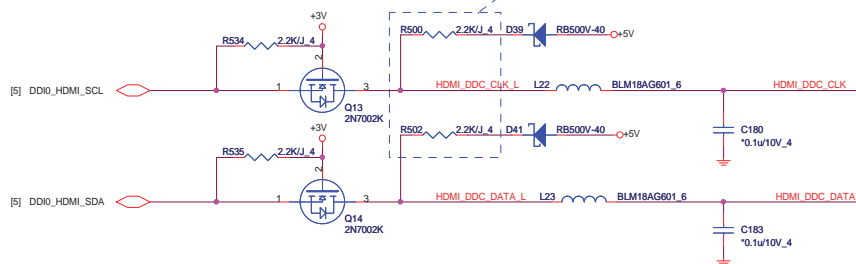
<201001001> Change from 100K to 1M ohm (follow DG0.7)

&lt;20101209&gt; Change to DFHS19FR015 by ME design change



## SDVO I2C Control (HDM)

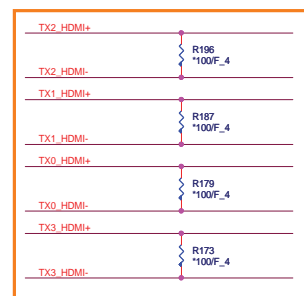
<20100909\_Jennifer> Change R500/ R502  
from 1.5k to 2.2k to follow CRB.



The DDC signals are rated at 5V at connector. The passgate can also be used to protect against back-power when computer is OFF but the display is ON and still pulled up to 5 V.

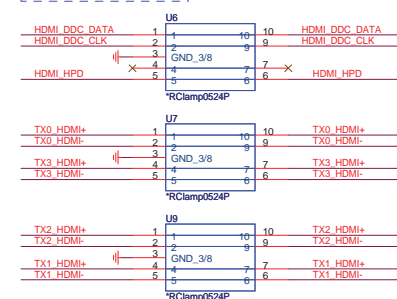
## EMI reserve for HDMI (EMC)

Close to HDMI Connector



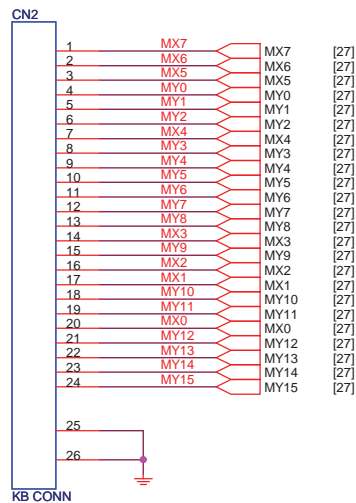
## ESD Protect (HDM)

Close to HDMI Connector

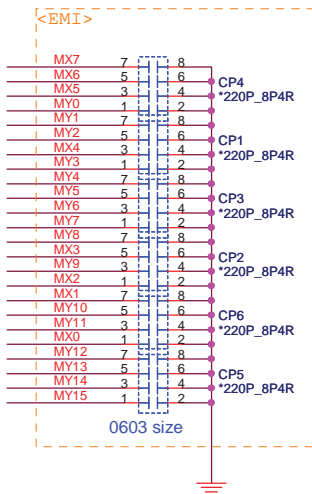




## KEYBOARD (KBC)

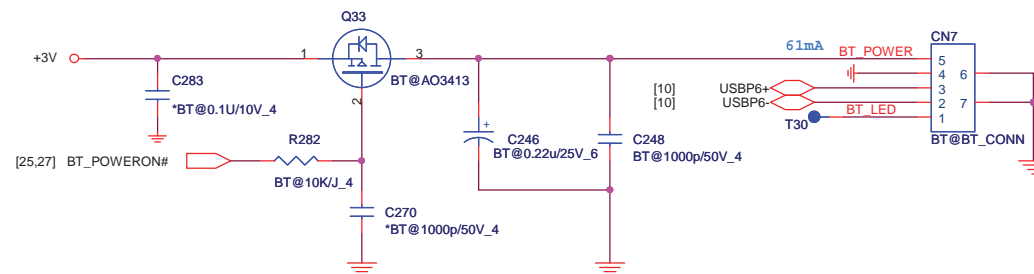


<20110214(E1A)>  
Change CP1~CP6 footprint from  
8p4r-0402-smt to 8P4R, for SMT open issue.

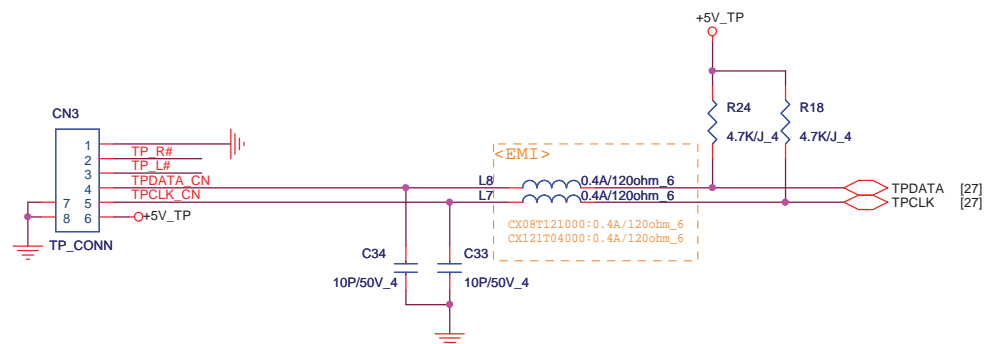


## BLUETOOTH (BTM)

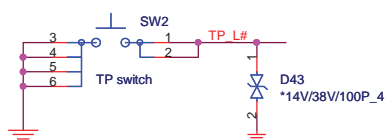
19



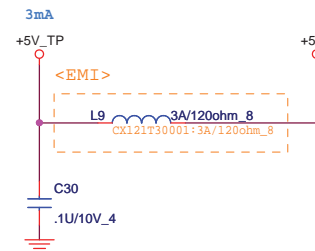
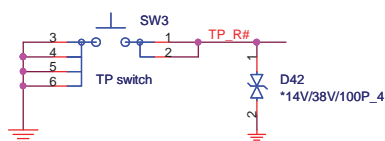
## TOUCH PAD (TPD)



### Left Button



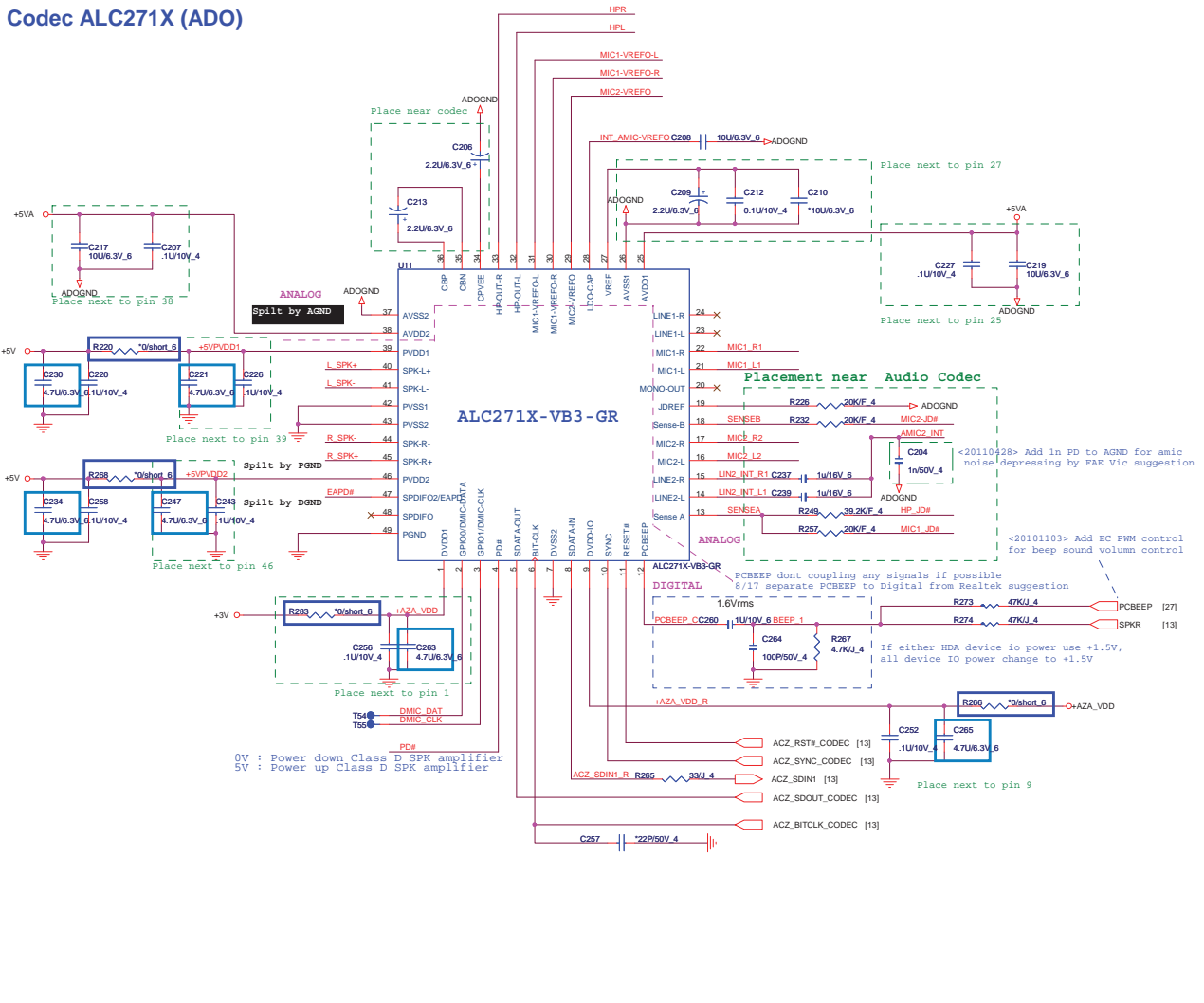
### Right Button



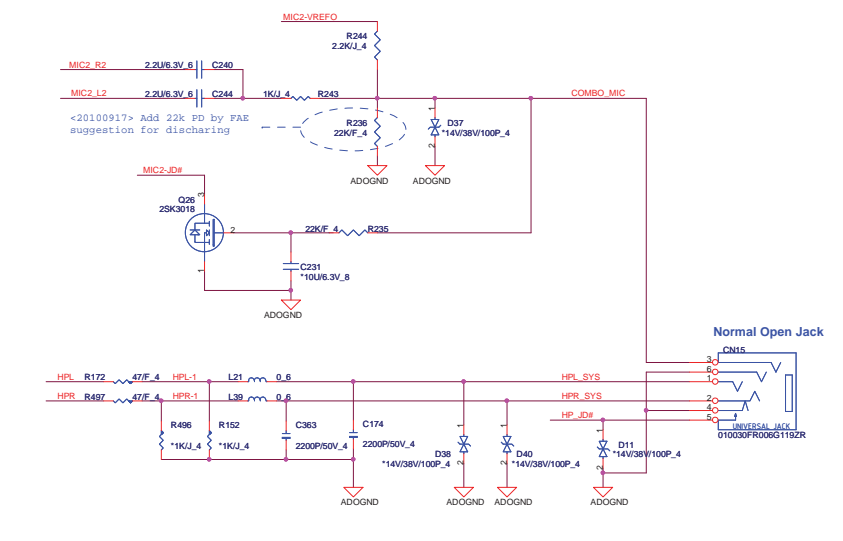
**Quanta Computer Inc.**  
**PROJECT : ZE7**

| Size  | Document Number                     | Rev            |
|-------|-------------------------------------|----------------|
|       | <b>KB/BT/TP/LED/Power Connector</b> | C3C            |
| Date: | Wednesday, August 31, 2011          | Sheet 19 of 42 |

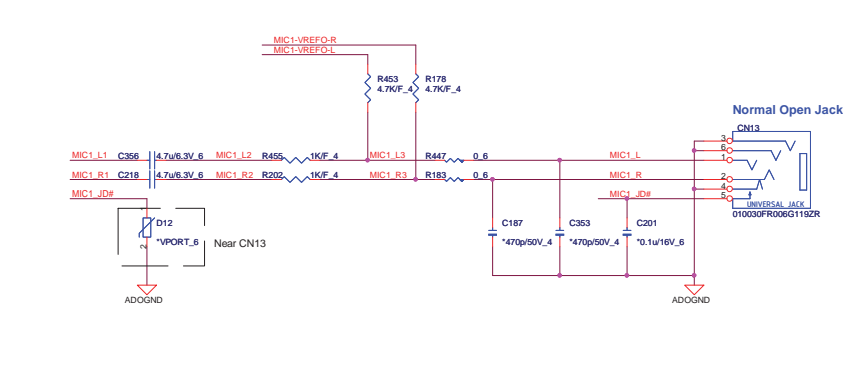
Codec ALC271X (ADO)



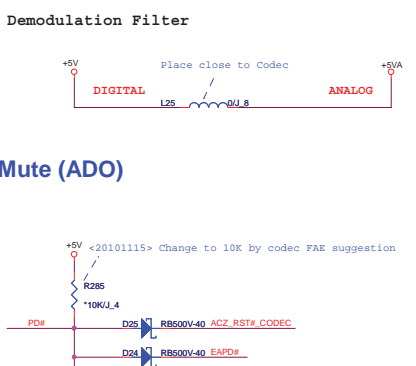
EARPHONE (AMP)



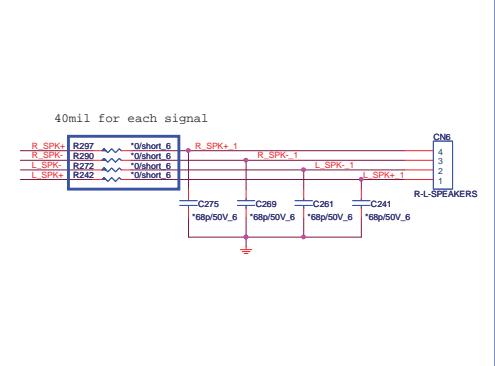
MIC (AMP)



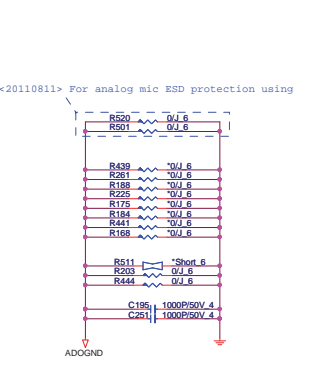
Power (ADO)



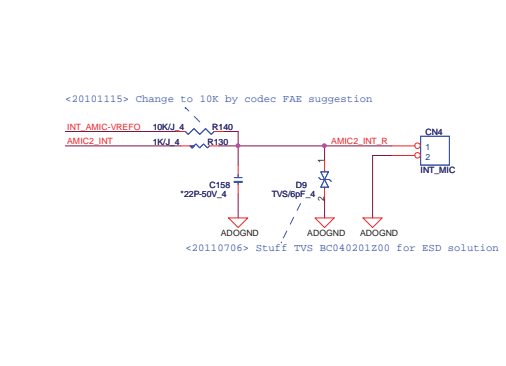
Internal Speaker (AMP)

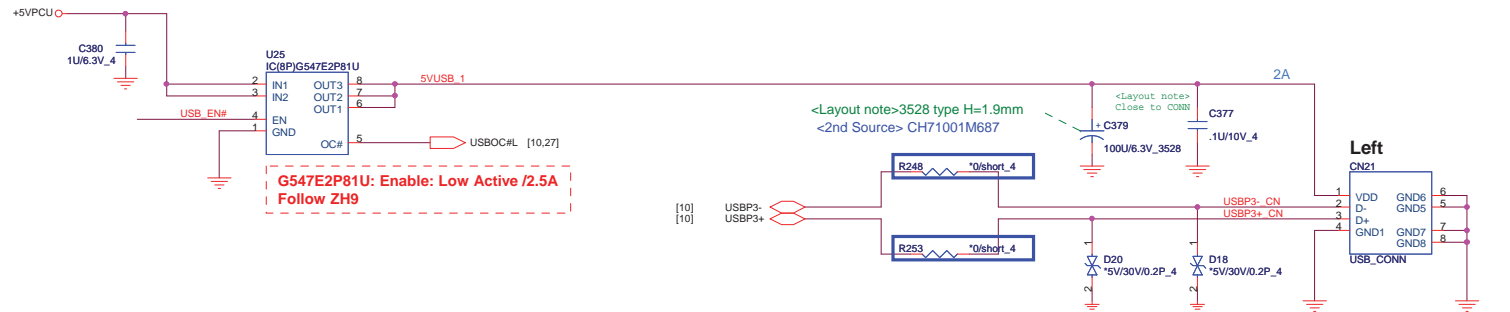


GND

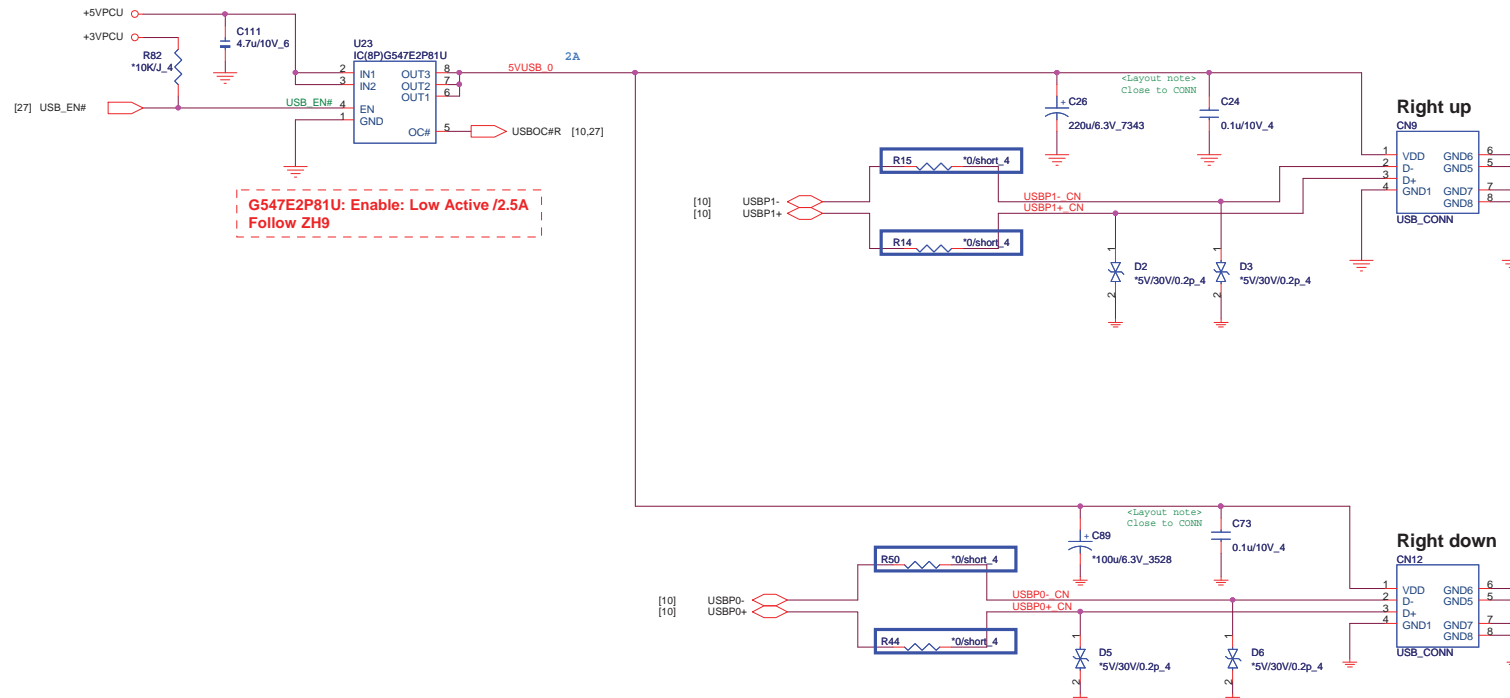


Internal Analog MIC (AMP)





## USB Right (USB)



Quanta Computer Inc.

PROJECT : ZE7

|      |                        |     |
|------|------------------------|-----|
| Size | Document Number        | Rev |
|      | USB Port/ MAX14566EETA | C3C |

Date: Wednesday, August 31, 2011 Sheet 21 of 42



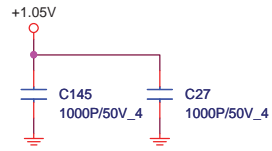
PROJECT : ZE7

|       |   |                |
|-------|---|----------------|
| Size  | Document Number<br><b>LAN RTL8105TA-VC-CG</b> | Rev<br>C3C     |
| Date: | Wednesday, August 31, 2011                    | Sheet 22 of 42 |

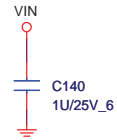
# Stitching Capacitor (CLG)

23

## For RF Request



## For CRT R/G/B Signals



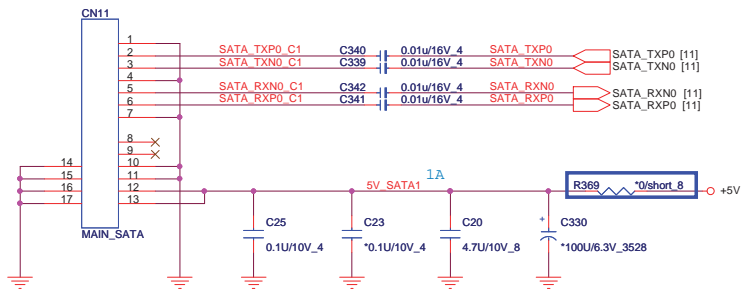
**Quanta Computer Inc.**

**PROJECT : ZE7**

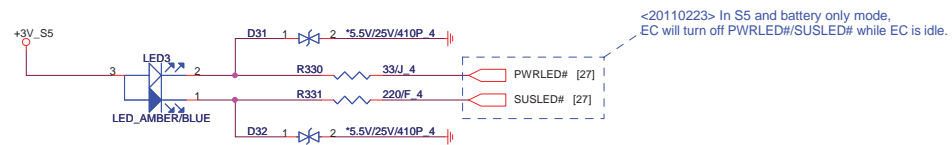
|      |                 |     |
|------|-----------------|-----|
| Size | Document Number | Rev |
|      |                 | C3C |

**Stitching Cap**

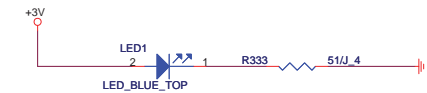
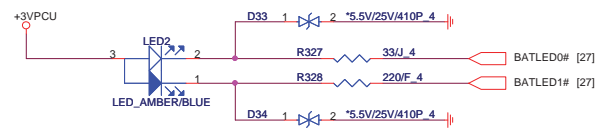
|       |                            |       |    |    |    |
|-------|----------------------------|-------|----|----|----|
| Date: | Wednesday, August 31, 2011 | Sheet | 23 | of | 42 |
|-------|----------------------------|-------|----|----|----|



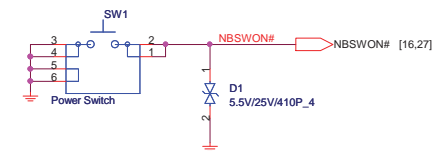
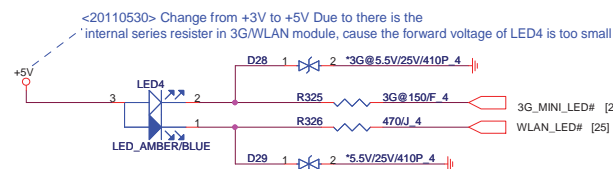
## LED/SW (UIF)

PWR LED  
SUS LED

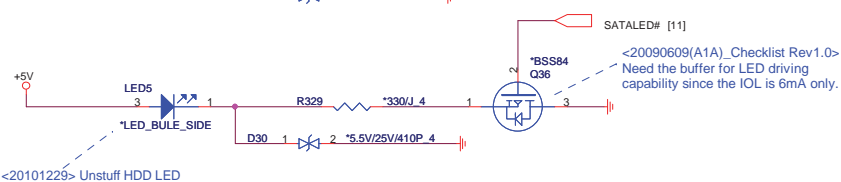
## PWR indicator

FULL LED  
CHG LED

## PWR button

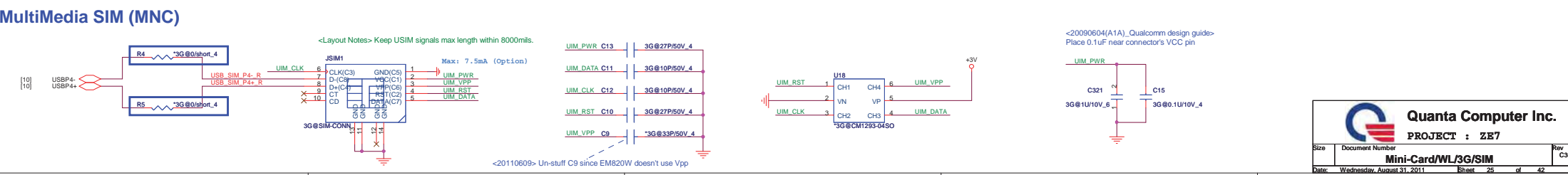
3G LED  
WLAN LED

## HDD LED



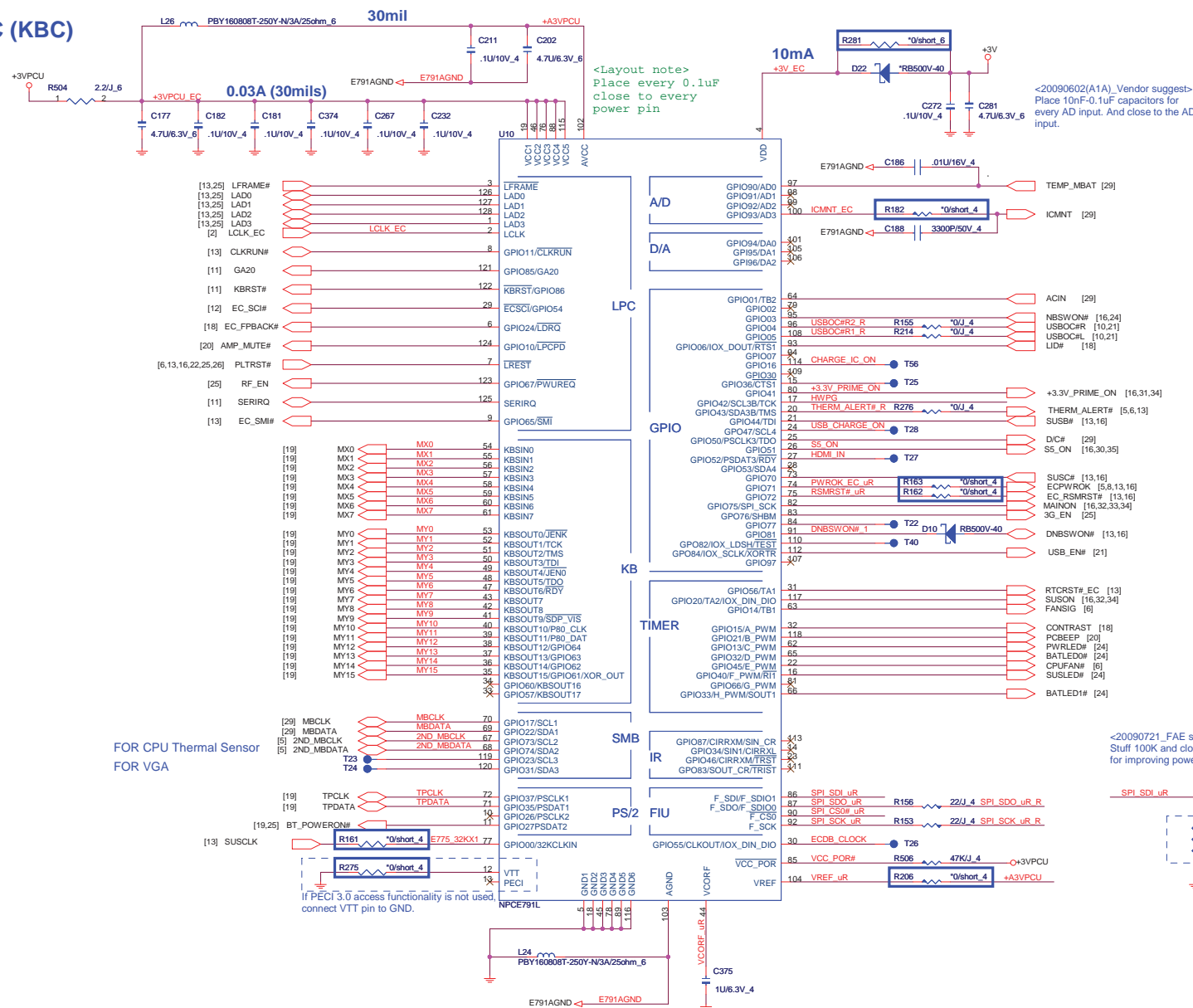
|               |                            |                      |          |
|---------------|----------------------------|----------------------|----------|
|               |                            | Quanta Computer Inc. |          |
| PROJECT : ZE7 |                            | Rev C3C              |          |
| Size          | Document Number            | SATA HDD/LED/SW      |          |
| Date          | Wednesday, August 31, 2011 | Sheet                | 24 of 42 |







## EC (KBC)



## I/O ADDRESS SETTING(KBC)

27

SHBM=0: Enable shared memory with host BIOS



1/13 Confirm by vendor mail :

Disabled ('1') if using FWH device on LPC.  
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

## SM BUS PU(KBC)



```
1ST: Battery
2ND: CPU Thermal Sensor / DTS
3RD: VGA Thermal Sensor
```



<20090831(A1A)\_EC team suggest>

- | 1.change R166/R167 to 1M or 100K ohm
- | 2.change PWR/SUS LED's power from +3VPCU to +3V\_S5 or +3VSUS
- | can reduce pull-high resistor of SUSLED#/PWRLED#

## SPI FLASH(KBC)

1/13 Confirm by vendor mail :

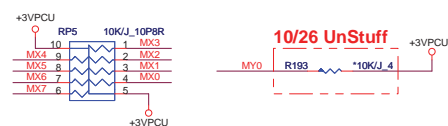
- l If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)



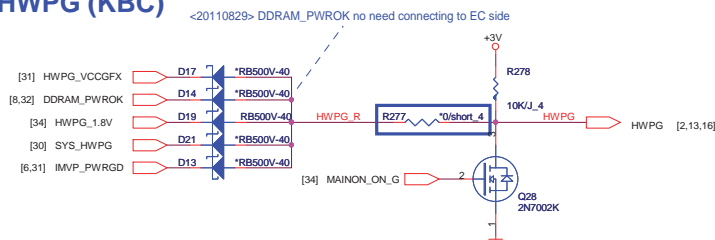
|                |                   |             |       |
|----------------|-------------------|-------------|-------|
| ZS9 A1~A3-test | W25Q16BVSSIG      | AKE38FP0N01 | 16M b |
| ZS9 A4-test    | W25Q16CVSSIG      | AKE38ZP0N02 | 16M b |
| ZS9 A5-test    | MX25L1606EM2I-12G | AKE38FP0Z01 | 16M b |
| ZS9 A6-test    | MX25L1606EM2I-12G | AKE38FP0Z01 | 16M b |
| ZS9 A7-test    | W25Q16BVSSIG      | AKE38FP0N01 | 16M b |

|         |                   |                               |
|---------|-------------------|-------------------------------|
| Winbond | W25Q16BVSSIG      | AKE38FP0N01                   |
| EON     | EN25F16-75HCP     | AKE38ZA0Q00                   |
| MXIC    | MX25L1606EM2I-12G | AKE38FP0Z01 (ZE6 MAC ID fail) |

## INTERNAL KEYBOARD STRIP SET (KBC)



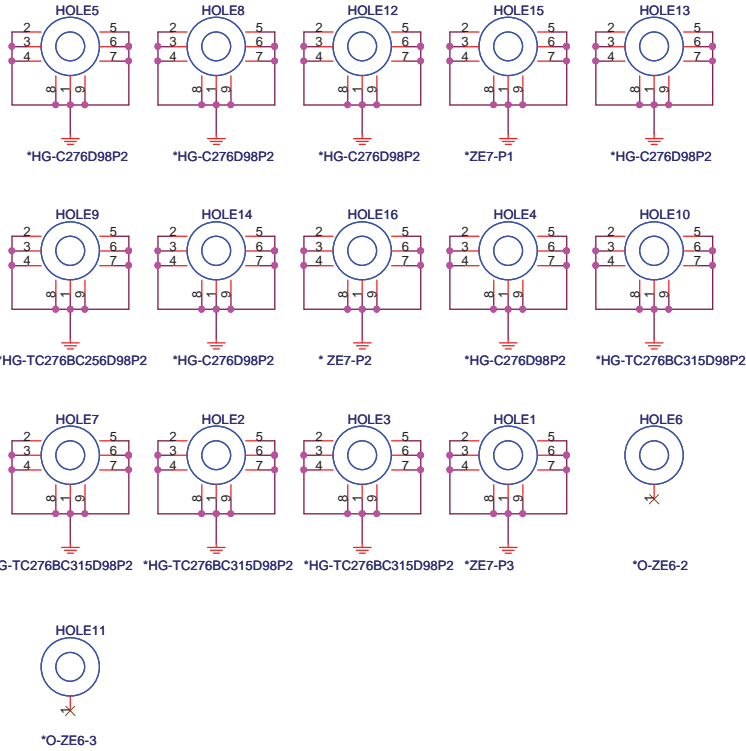
## HWPG (KBC)

|  $\leq \text{FMT}$  |

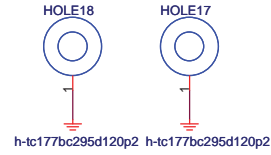
# HOLE (OTH)

28

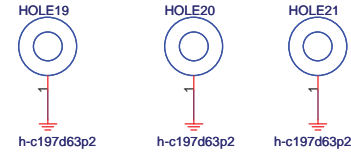
## TOP(HDD Hole)



## BOT(Thermal Hole)



## BOT(Mini-PCle Hole)



## LED ESD PAD



## TP ESD PAD

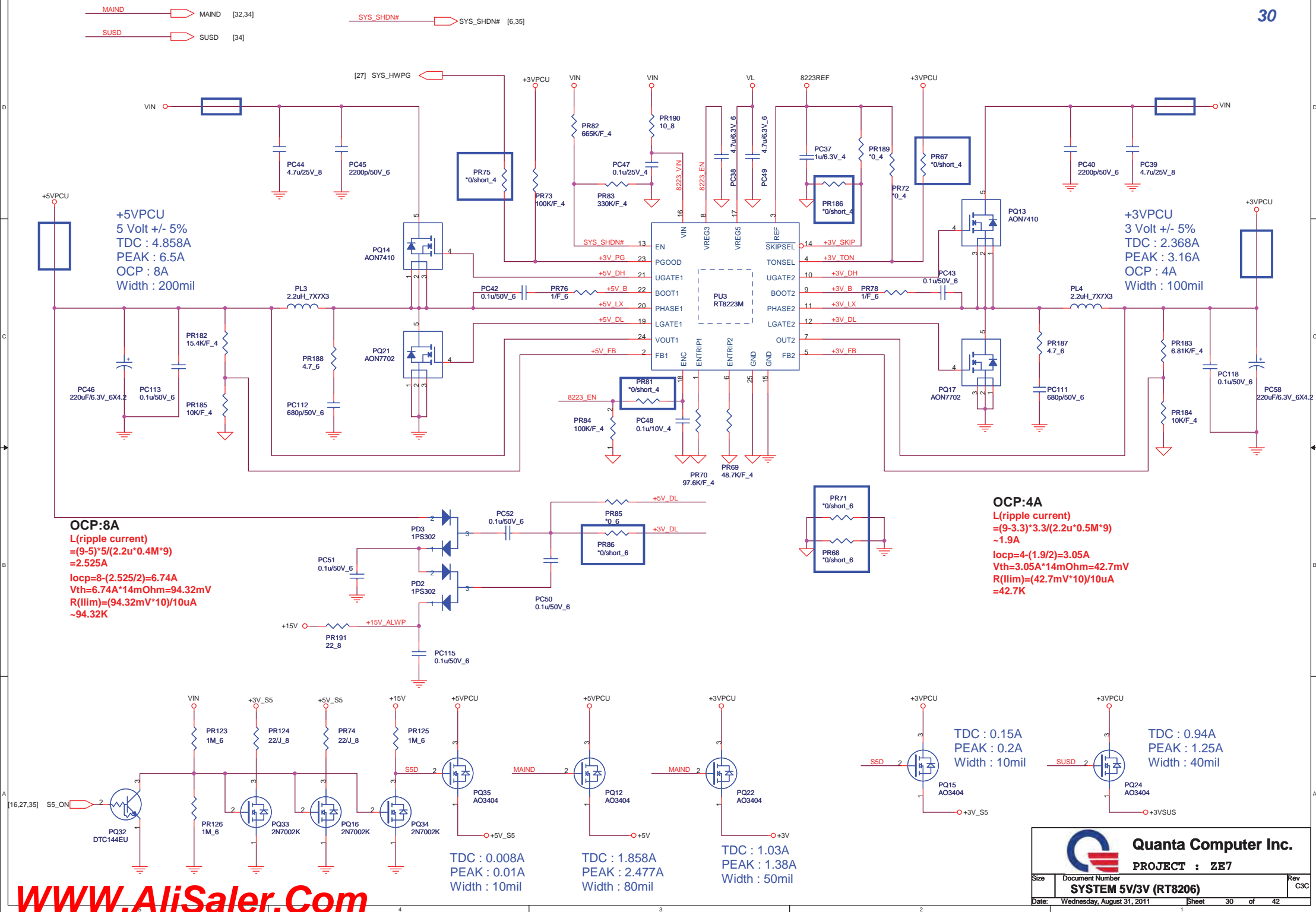


Quanta Computer Inc.

PROJECT : ZE7

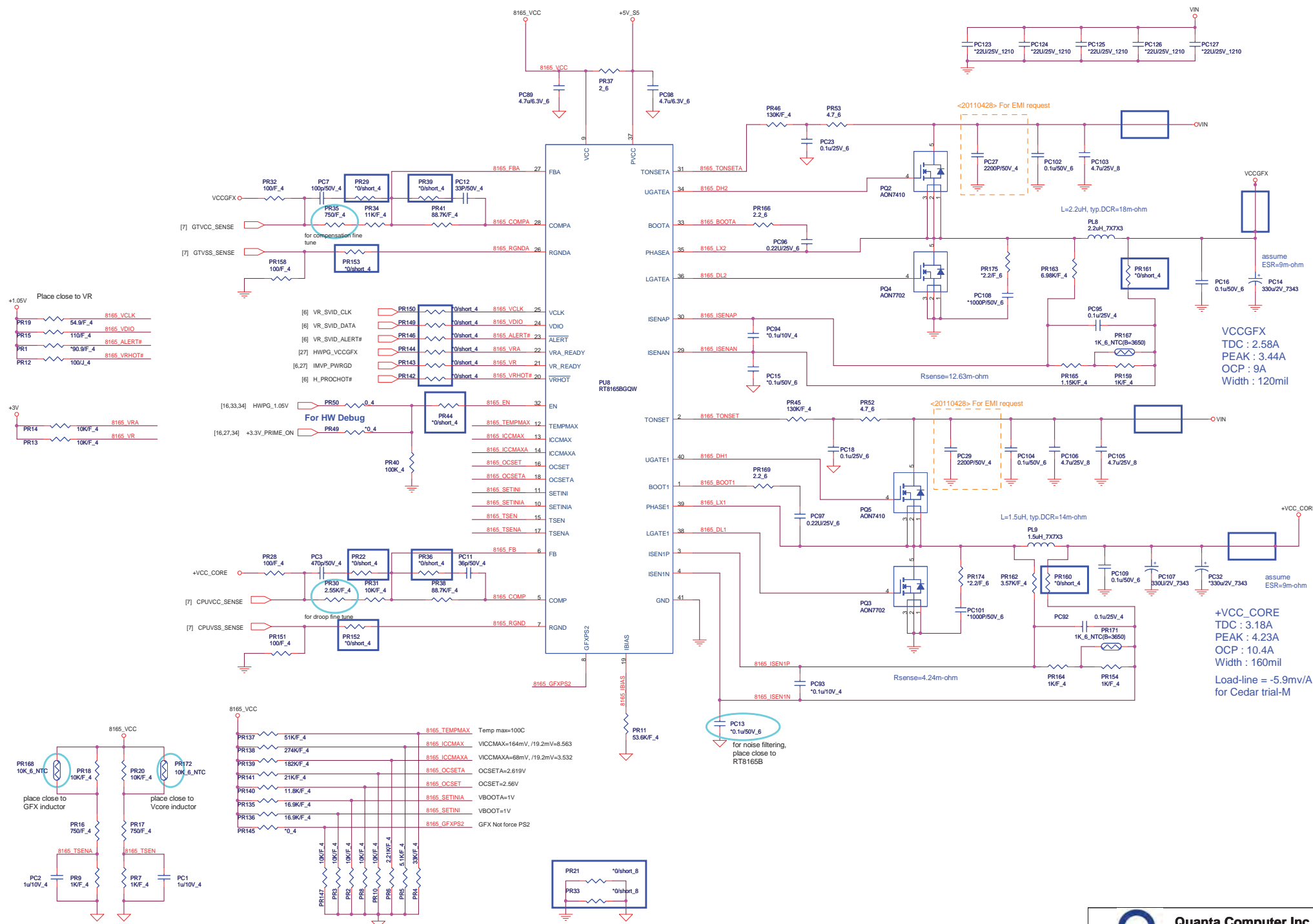
|       |                            |                |
|-------|----------------------------|----------------|
| Size  | Document Number            | Rev            |
|       | EMI/Hole                   | C3C            |
| Date: | Wednesday, August 31, 2011 | Sheet 28 of 42 |



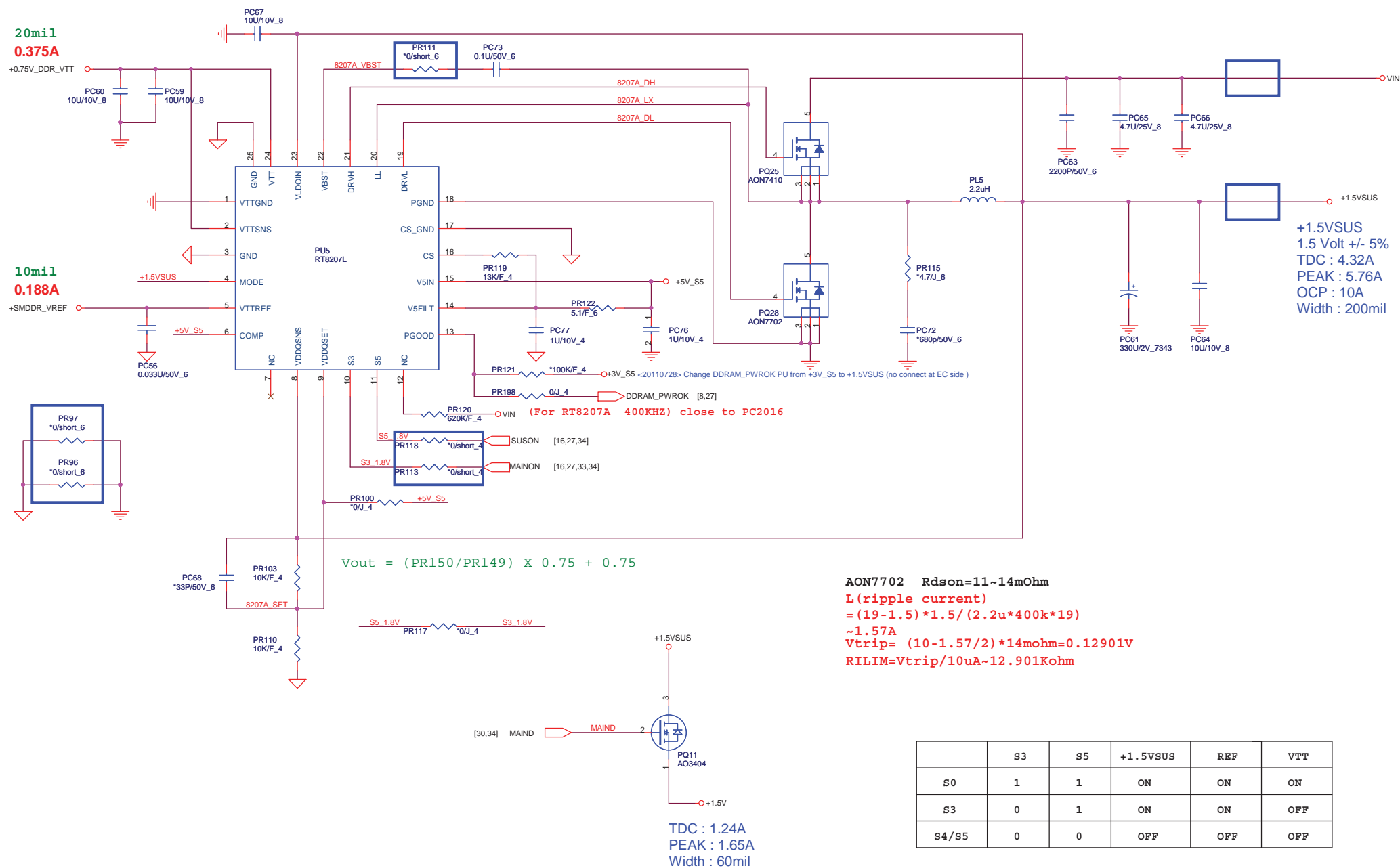


**Quanta Computer Inc.**  
**PROJECT : ZE7**

| Size  | Document Number              | Rev            |
|-------|------------------------------|----------------|
|       | <b>SYSTEM 5V/3V (RT8206)</b> | C3C            |
| Date: | Wednesday, August 31, 2011   | Sheet 30 of 42 |



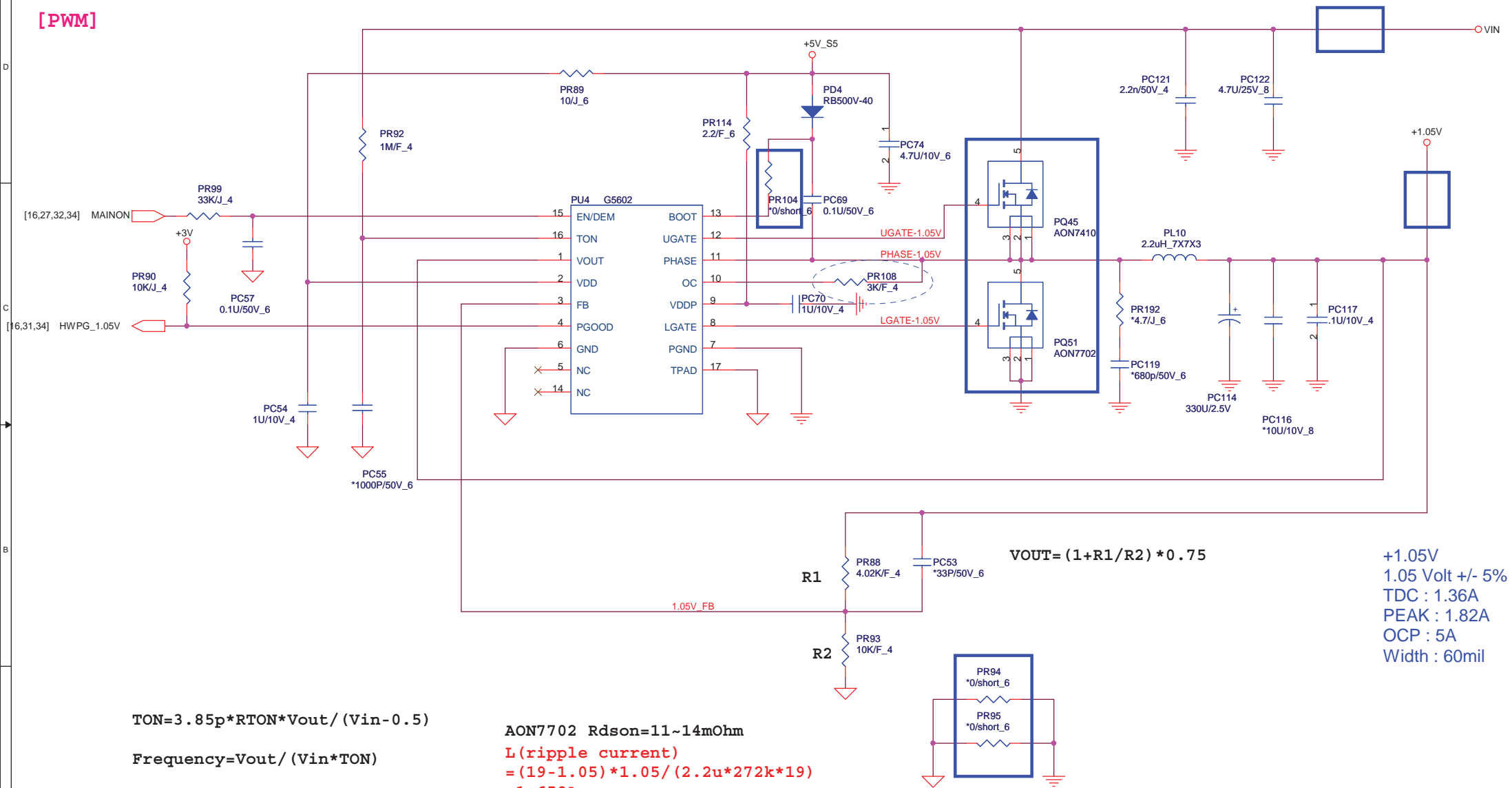
[PWM]



|       | S3 | S5 | +1.5VSUS | REF | VTT |
|-------|----|----|----------|-----|-----|
| S0    | 1  | 1  | ON       | ON  | ON  |
| S3    | 0  | 1  | ON       | ON  | OFF |
| S4/S5 | 0  | 0  | OFF      | OFF | OFF |



[PWM]

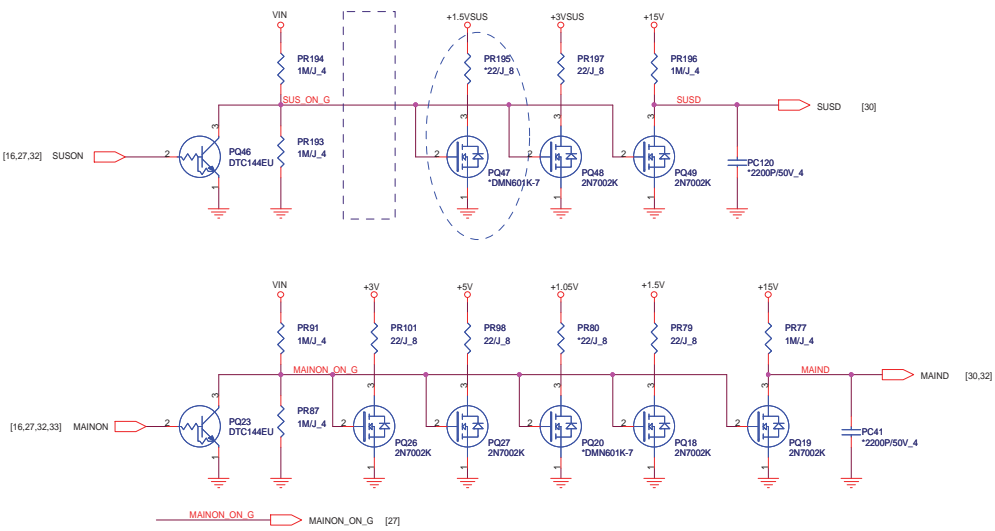


Quanta Computer Inc.

PROJECT : ZE7

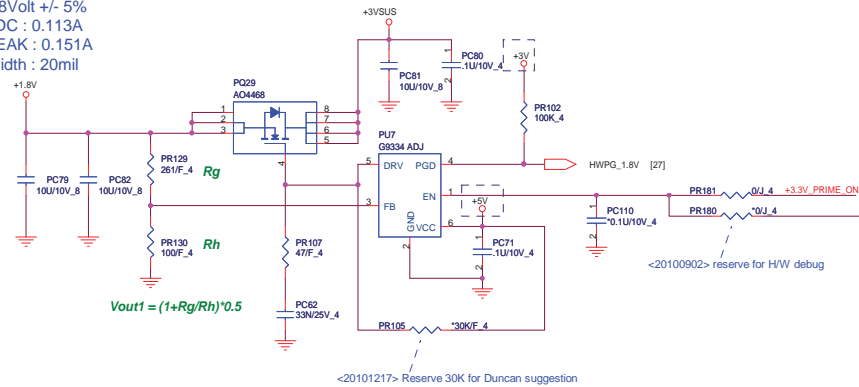
|      |                           |     |
|------|---------------------------|-----|
| Size | Document Number           | Rev |
|      | <b>+1.05V(UP6111AQDD)</b> | C3C |

Date: Wednesday, August 31, 2011 Sheet 33 of 42

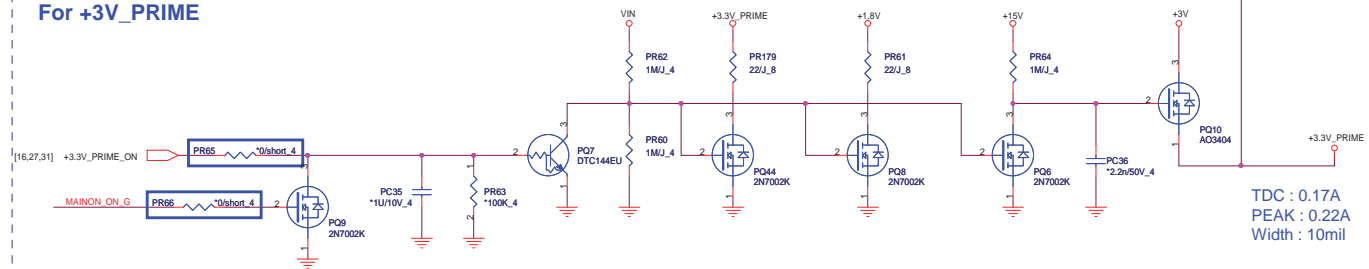


### Reserve For VCCGFX

+1.8V  
1.8Volt +/- 5%  
TDC : 0.113A  
PEAK : 0.151A  
Width : 20mil



### For +3V\_PRIME



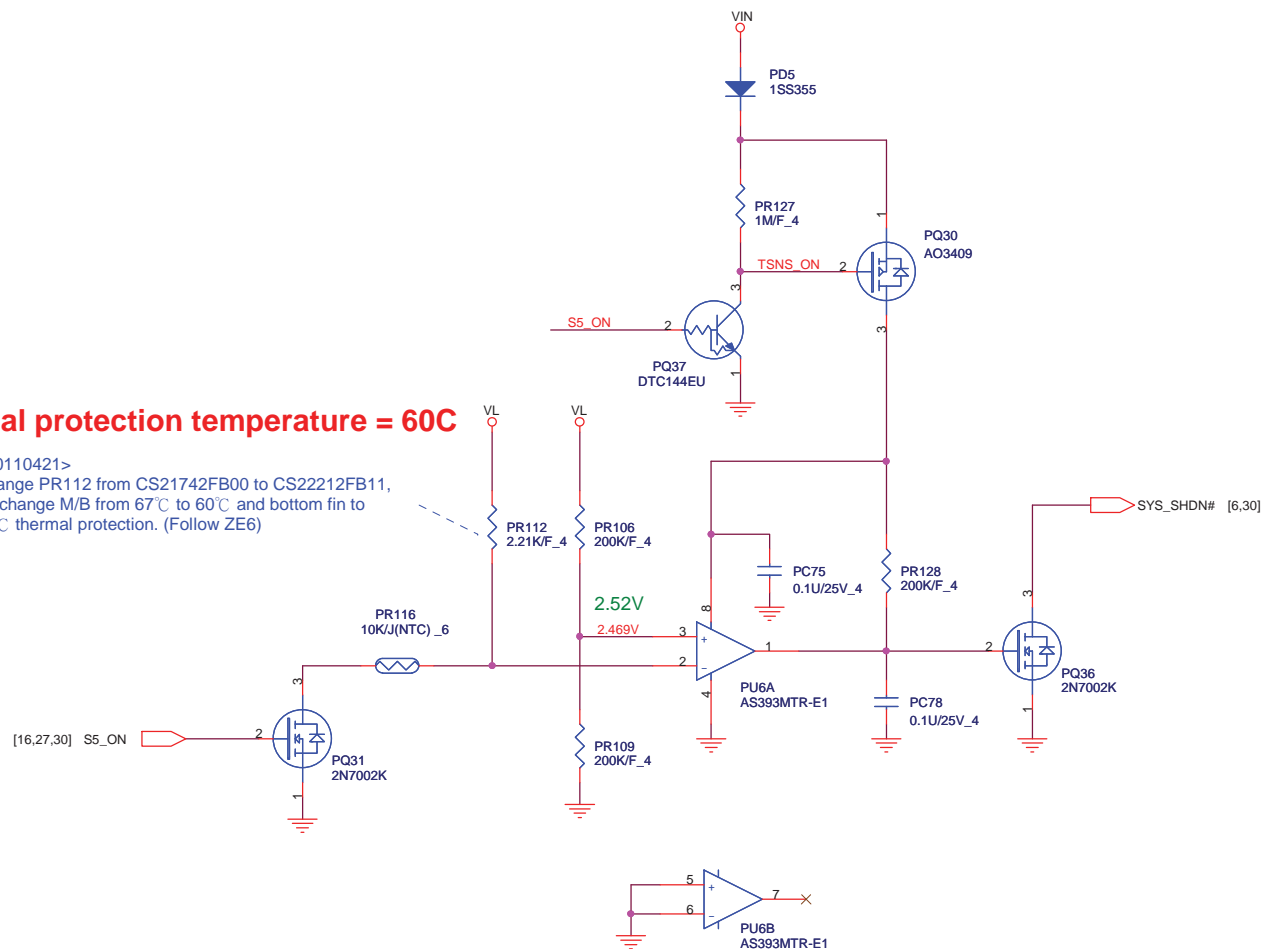
**Quanta Computer Inc.**  
PROJECT : ZE7

# Thermal Protection (DCD)

**Thermal protection temperature = 60C**

<20110421>

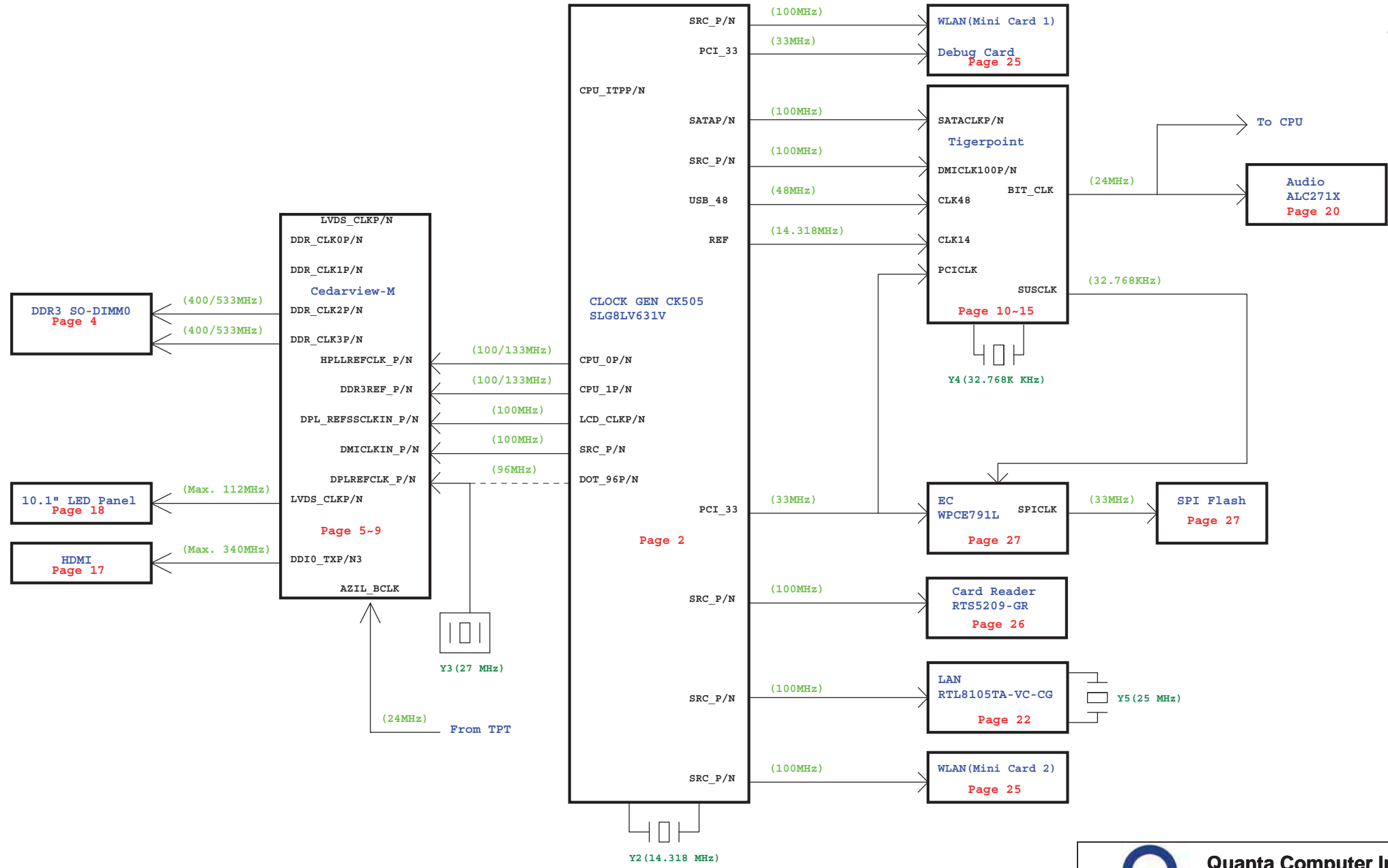
Change PR112 from CS21742FB00 to CS22212FB11,  
for change M/B from 67°C to 60°C and bottom fin to  
88°C thermal protection. (Follow ZE6)



**Quanta Computer Inc.**

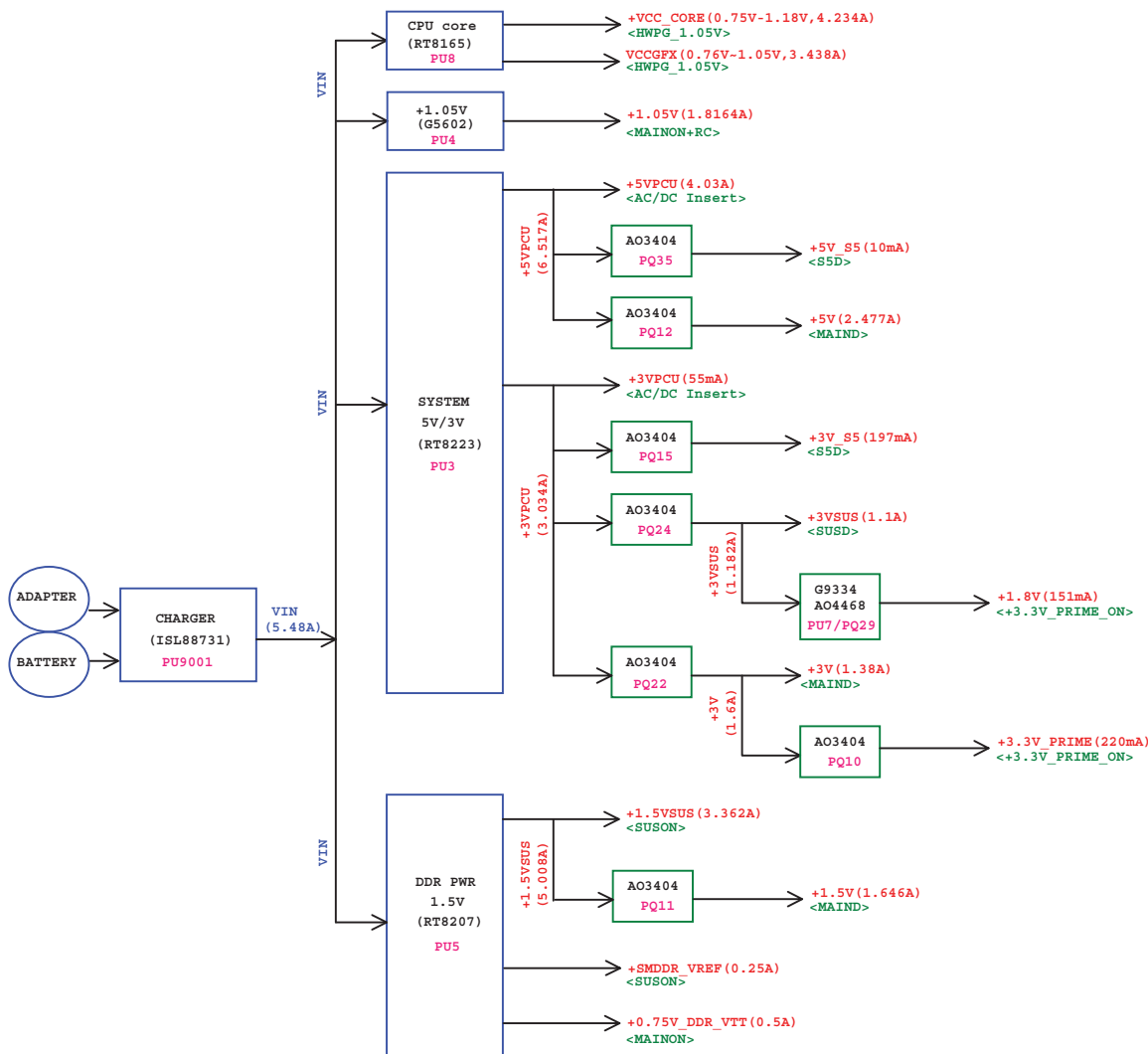
**PROJECT : ZE7**

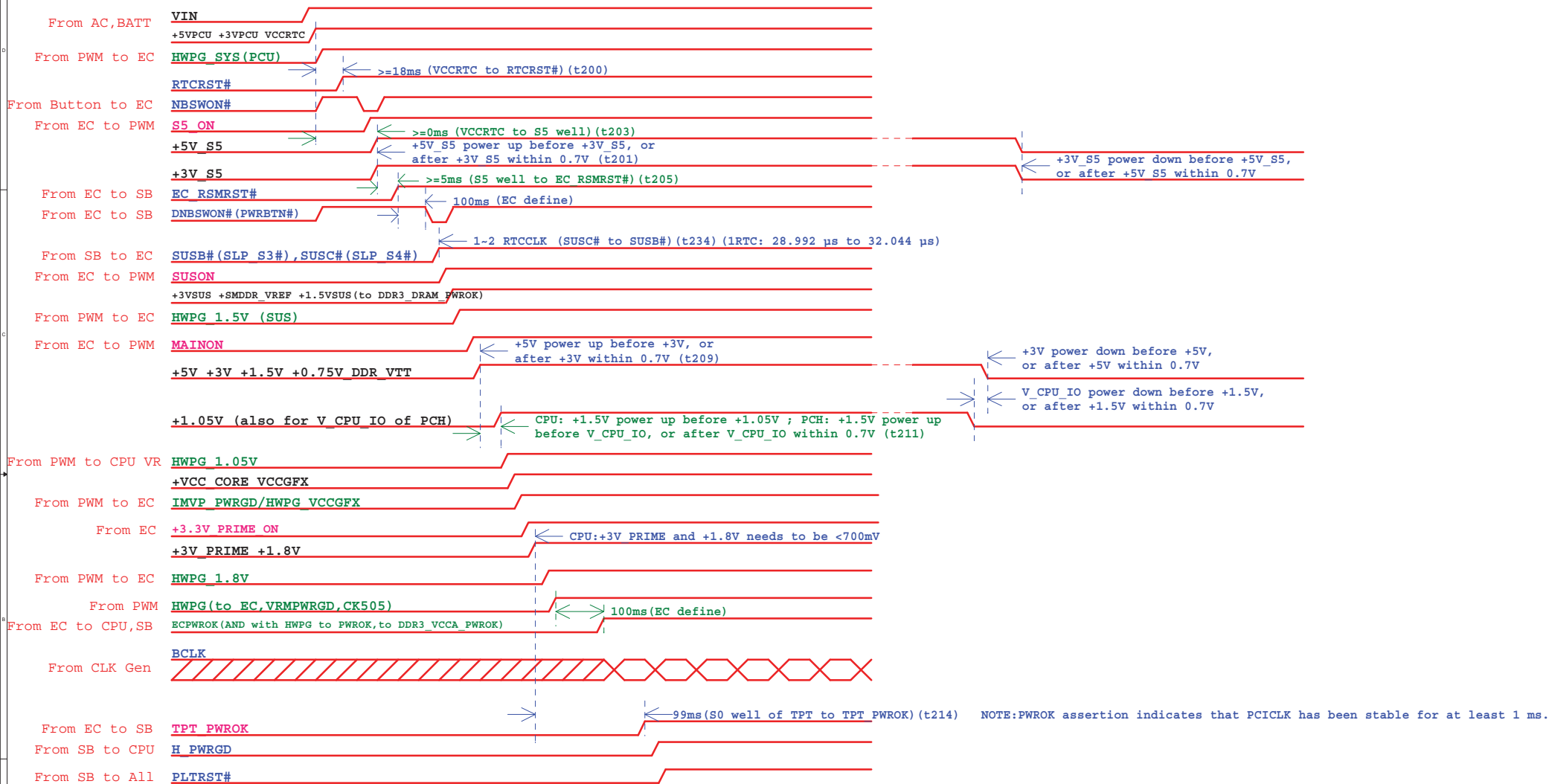
|       |                            |                |
|-------|----------------------------|----------------|
| Size  | Document Number            | Rev            |
|       | <b>Thermal protect</b>     | C3C            |
| Date: | Wednesday, August 31, 2011 | Sheet 35 of 42 |



## BOM Structure

|              | Function  | Description               |  |
|--------------|-----------|---------------------------|--|
| 3G           | 3G@       | w/ 3G module              | stuff 3G@  |
|              |           | w/o 3G module             | unstuff 3G@  |
| BT           | BT@       | w/ BT module              | stuff BT@  |
|              |           | w/o BT module             | unstuff BT@  |
| LVDS/EDP     | LVDS@     | w/ LVDS (default)         | stuff LVDS@<br>L38: CV+1003JN01 (0.1UH)<br>C334: CH5102K9B06 (1UF) |
|              | EDP@      | w/ EDP                    | stuff EDP@<br>L38: CS00003J951 (0ohm)<br>C334:CS00002JB38 (0ohm)   |
| Deep Standby | DS3@      | w/ deep standby (default) | stuff DS3@   |
|              | NS3@      | w/ normal standby         | stuff NS3@   |
| PLL Power    | 1.5VPLL@  | w/ 1.5VPLL (default)      | stuff 1.5VPLL@   |
|              | 1.05VPLL@ | w/ 1.05VPLL               | stuff 1.05VPLL@  |
|              |           |                           |  |





\*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

|                               | CLK GEN | RAM   | *Mini Card (WLAN) | *XDP  |  |
|-------------------------------|---------|-------|-------------------|-------|--|
| (SMB_DATA)/(SMB_CLK) (+3V_S5) | V       | V     | V                 | V     |  |
| Power Plane                   | +3V     | +3V   | +3V               | +3V   |  |
| MOS CKT (Level shift)         | Stuff   | Stuff | Stuff             | Stuff |  |

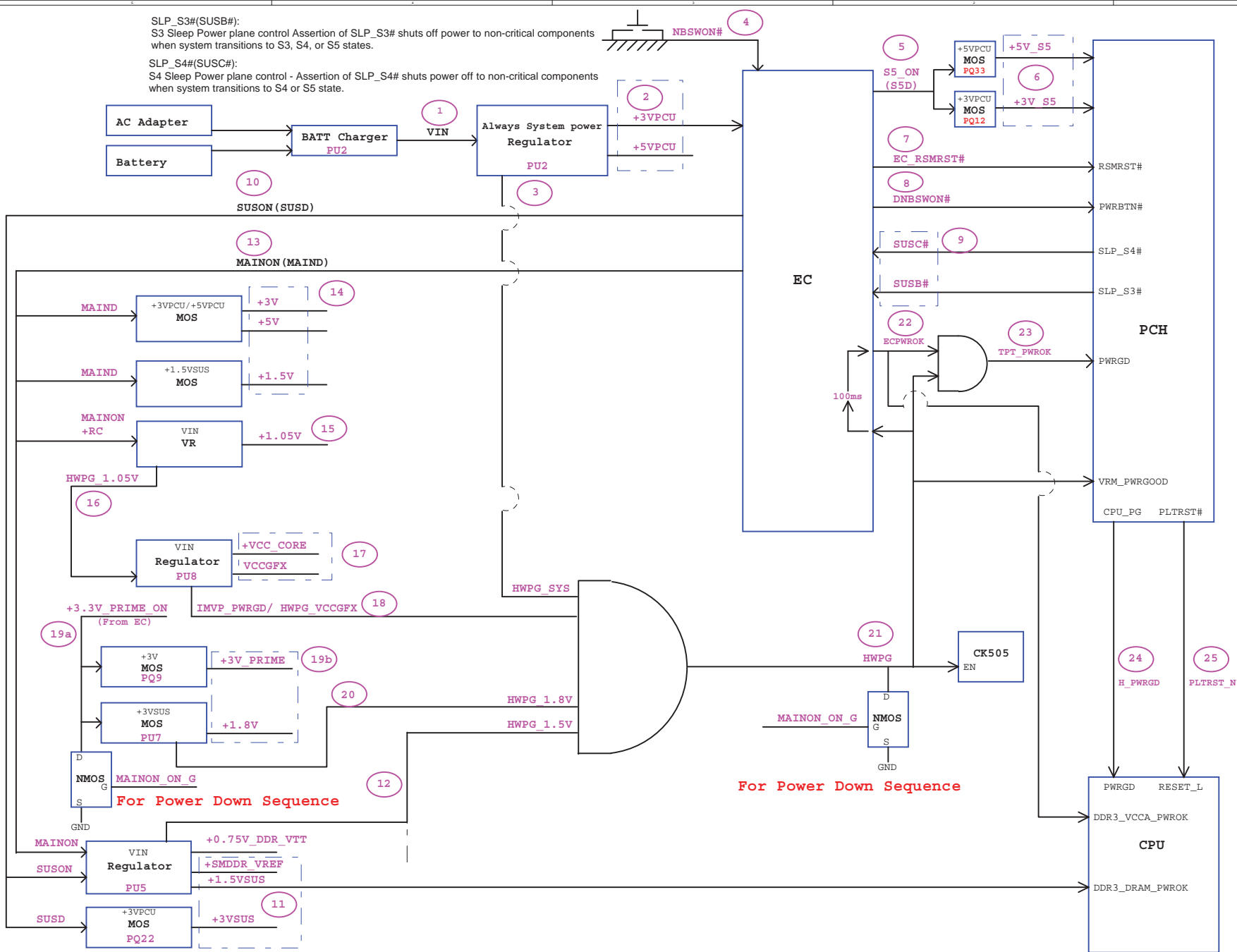
\*=Reserve

EC SMBUS Table

|                            | Battery | CPU Thermal Sensor | GFX Thermal Sensor |
|----------------------------|---------|--------------------|--------------------|
| EC791 SDA1 / SCL1 (+3VPCU) | V       |                    |                    |
| EC791 SDA2 / SCL2          |         |                    |                    |
| EC791 SDA3 / SCL3          |         |                    |                    |
| Power Plane                | +3VPCU  |                    |                    |
| MOS CKT (Level shift)      | X       |                    |                    |


SLP\_S3#(SUSB#):  
S3 Sleep Power plane control Assertion of SLP\_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP\_S4#(SUSC#):  
S4 Sleep Power plane control - Assertion of SLP\_S4# shuts power off to non-critical components when system transitions to S4 or S5 state.



| Model  | REV |  | CHANGE LIST  | MODEL | ZE7  |     |
|--------|-----|--|--|-------|------|-----|
|        |     |  |  |       | FROM | To  |
|        |     |  |  |       | C1A  | D1A |
| ZE7 MB | DIA |  | 20101124: <Page 27> Del net USB_EN#_1 / USB_EN#_2 / USBOC#R2 / USBOC#R1 / 5VUSB_3<br><Page 27> Add USB_EN# / USBOC#R<br><Page 10> Del USBOC0# / USBOC3# / USBOC1# ; Add USBOC#R_1 / USBOC#L_1<br><Page 26> Add net SD_D2_R   |       |      |     |
|        |     |  | 20101125: <Page 26> Del net MS_CLK_R / PCIE_CLK_REQ1#<br><Page 26> Delete R628; Reserve C510 for EMI (follow vendor CRB)   |       |      |     |
|        |     |  | 20101126: <Page 5> Add net name TX1_HDMI+ / TX1_HDMI- / TX2_HDMI+ / TX2_HDMI- / TX3_HDMI+ / TX3_HDMI-<br><Page 5> Add net name TXLOUT0_R+ EDPTX1+ / TXLOUT0_R- EDPTX1- / TXCLKOUT+_R EDPTX2+ / TXCLKOUT-_R EDPTX2-<br><Page 5> Add net name LCD_CLK_R EDPTX3+ / LCD_DATA_R EDPTX3-   |       |      |     |
|        |     |  | 20101129: <Page 27> Change UI4 from AKE38FP0N01 to AKE38ZP0N02 for EC request<br><Page 20> Modify Headphone Jack schematic to follow ZE6<br><Page 24> Add LED5 for power indicator   |       |      |     |
|        |     |  | 20101130: <Page 16> Delete SIO board connector<br><Page 5> Stuff C432 to follow checklist0.7<br><Page 7> Stuff C422; Unstuff C210/C111; Change C408 to 22U/6.3V_8/ C409 to 1U/6.3V_4 to follow checklist0.7  |       |      |     |
|        |     |  | 20101206: <Page 26> Change card reader connector F/N footprint due to ME request<br><Page 29> Update battery connector to follow ZE6   |       |      |     |
|        |     |  | 20101209: <Page 17> Change HDMI connector to DFHS19FR015 by PDC suggestion   |       |      |     |
|        |     |  | 20101213: <Page 31> Delete PC120 at +VCC_CORE (Power team Duncan will use A3 M/B to verify again)<br><Page 18> Reserve L21/ L22 /L40 /L41/ R253/ R258/ R259/ R262/ R263/ R265/ R269 for LVDS signals (RF suggestion)   |       |      |     |
|        |     |  | 20101216: <Page31> Reserve PC53/PC120 for EMI suggestion<br><Page12> Reserve R356/ C290 for EMI suggestion   |       |      |     |
|        |     |  | 20101217: <Page20> Change CN10(internal speaker CONN) from DFHD04MR981 to DFHD04MRA75 (follow ZE6)<br><Page28> Add NUT part number (follow ZE6)  |       |      |     |
|        |     |  | 20101220: <Page5> Swap DDI0_TX2_DP /DDI0_TX0_DP ; Swap DDI0_TX2_DN /DDI0_TX0_DN to correct HDMI channel<br><Page22> Change RJ45 connector to DFTJ12FR221 to follow ZE6   |       |      |     |
|        |     |  | 20101221: <Page13> Change RTC battery from pin type to holder(DFHS02FS561)   |       |      |     |
|        |     |  | 20101228: <Page29-35> Update power budget description<br><Page1-40> Update test pad size to TP2650<br><Page29> Update battery connector P/N to DFAD08MR013 (follow ZE6)  |       |      |     |
|        |     |  | 20101229: <Page24> Unstuff HDD LED related circuit for cost down requirement<br><Page31> Change PR71 to 5.72K_F cause VCCGFX power-budget has changed to 2.58A (Power budget V0.3)<br><Page20> Modify speaker connector pin definition to follow PDC design  |       |      |     |
|        |     |  | 20101231: <Page20> Modify earphone and mic connector pin definition  |       |      |     |
|        |     |  | 20110103: <Page22> Modify CLKREQ_LAN#_R to CLKREQ_LAN#_R1 because netname duplicate  |       |      |     |
|        |     |  | 20110104: <Page13> Change EC_SMI# to GPIO10; Delete net PCH_GPIO10; Add net PCH_GPIO8<br><Page20> Modify speaker connector pin definition back to original design<br><Page19> Modify TP connector pin define to correct TP doesn't work issue<br>--Gerber out for A4-test--  |       |      |     |
|        |     |  | 20110105: <Page 25> Add net WLAN_LED1#   |       |      |     |
|        |     |  | 20110106: <Page 7> Change L8/ L12/ L13 from CV01001MN16 to CV01001MN08 for shortage issue  |       |      |     |
|        |     |  | 20110107: <Page 5> Add NCT7717U thermal sensor circuit (Reserve)   |       |      |     |
|        |     |  | 20110110: <Page 2> Add R515/ R516 for USB 48M CFG input hardware strapping to allocate PLL assignment. (Reserve)<br><Page 10> Exchange USB port1 with port3 for S3 auto resume issue   |       |      |     |
|        |     |  | 20110111: <Page 21> Add USBP3- L1/ USBP3+ L1/ USBP3- L2/ USBP3+ L2/ USBP3- L/ USBP3+ L/ CHARGE_IC_ON for USB charger reserve<br><Page 20> Add net AMIC2 INT; Delete net LIN2 INT R/ LIN2 INT L for A-MIC (follow ZE6)  |       |      |     |
|        |     |  | 20110113: <Page 27> Add DNBSWON#_1 and D41 to solve +3V_S5 current leakage   |       |      |     |
|        |     |  | 20110117: <Page 20> Reverse CN4 connector routing for A-MIC cable design (follow ZE6)  |       |      |     |
|        |     |  | 20110119: <Page 2> Change R515 from 10K ohm to 20K ohm for vendor's suggestion. (Reserve)  |       |      |     |
|        |     |  | 20110124: <Page 25> Change net name from CLKREQ_NMC# to CLKREQ_3G#<br><Page 25> Change R257 from 10K to 100K to solve leakage (follow ZE6)   |       |      |     |
|        |     |  | 20110127: <Page 18> Delete netname VCC_DDC   |       |      |     |
|        |     |  | 20110214: <Page 19> Change CPl-CP6 footprint from 8p4r-0402-smt to 8P4R for SMT open issue   |       |      |     |
|        |     |  | 20110221: <Page 2> Reserve 0.1F cap to solve that PCICLK (EC 33MHz) sometimes will change to 25MHz after flash BIOS and restart in first time issue.<br><Page 2> Exchange PCLK_DEBUG and LCLK_EC for PCICLK issue.   |       |      |     |
|        |     |  | 20110224: <Page 18> Change C300 from 2.2U to 10U to solve LCDVCC fall time issue.<br><Page 18> Add net +5V_LCD for IVO panel using<br><Page 20> Reserve DMIC signals to co-layout with DMIC connector, reserve R526/ R527 add net AMICINT_DMICDAT / AMICGND_DMICCLK<br><Page 10> Unstuff C111/ C123/ C125/ C133/ R78/ R79/ R84/ R86 to change DMI from x4 to x2  |       |      |     |
|        |     |  | 20110301: <Page 07> Change C326 from 10U to 47U; Add C386 47U for CRT flickr issue.<br><Page 18> Change L15/ L16/ L17 from 47ohm to 22ohm; Remove C109/ C110/ C114 for CRT issue<br><Page 18> Change C79/ C80/ C81 from 22pF to 4.7pF for CRT issue.   |       |      |     |
|        |     |  | 20110302: <Page 35> Reserve PR129 for no use   |       |      |     |
|        |     |  | 20110303: <Page 5> Reserve DDI1_PU resistors R529 to follow CRB(eDP); Add net DDI1_DDC_SCL/ DDI1_DDC_SDA<br><Page 20> Reserve L42/ L43/ L44/ L45 for ESD solution  |       |      |     |
|        |     |  | 20110304: <Page 20> Change R525 from 0603 short pad to 0603 0ohm<br><Page 25> Unstuff PD8/ PR106/ PR133 for no use<br><Page 5> Stuff R512/ R513/ U26/ C381/ C382/ R514/ R509/ C384/ C383 for thermal sensor<br><Page 27> Stuff R175/ R160 for thermal sensor<br><Page 24> Unstuff C320 for cost down   |       |      |     |
|        |     |  | 20110307: <Page 18> Reserve R530 for eDP function hardware short term solution   |       |      |     |
|        |     |  | 20110308: <Page 23> Reserve stitching cap for RF suggestion<br><Page 24> Unstuff C320 for cost down<br><Page 35> Delete PR106/ PR113/ PD8/ PR129 (thermal protection) for unused circuit (follow ZYG)<br><Page 28> Change Hole16/ Hole17 footprint to h-tcl77bc295d120p2<br><Page 5> Delete R510/ R511 for thermal sensor SMBUS_PU (PU at EC side)<br><Page 5> Unstuff C384/ C383; Change C382 from 10U_8 to 4.7U_6<br><Page 6> Reserve R531 for thermal sensor test |       |      |     |

|              |                 |     |              |       |  |
|--------------|-----------------|-----|--------------|-------|--|
| DOC NO.      | PROJECT MODEL : | ZE7 | APPROVED BY: | DATE: |  |
| PART NUMBER: | DRAWING BY:     |     | REVISION:    |       |  |


**Quanta Computer Inc.**  
**PROJECT : ZE7**

Size Document Number  
**Change List1**  
 Date: Wednesday, August 31, 2011 Sheet 40 of 42


Rev C/C



| Model  | REV | CHANGE LIST   | MODEL | ZE7  |     |
|--------|-----|---|-------|------|-----|
|        |     |   |       | FROM | To  |
| ZE7 MB | E1A | 20110308: <Page 13> Unstuff R451 for using thermal sensor (Need stuff when no use thermal sensor)<br><Page 27> Change thermal sensor SMBUS PU from +3V_S5 to +3V<br><Page 28> Change Hole18/ Hole19/ Hole20 footprint to h-c197d63p2<br><Page 18> Add R510 for eDP function verifying   |       | C1A  | D1A |
|        |     | 20110309: <Page 28> Add hole23<br><Page 20> Change R525 from 0603 short pad to 0402 0ohm<br>--Gerber out for A5-test--  |       | D1A  | E1A |
|        | F1A | 20110309: <Page 20> Change R525 from 0603 short pad to 0402 0ohm  |       | E1A  | F1A |
|        |     | 20110314: <Page 27> Change U7(BIOS) to AKE38FP0Z01 (follow ZE6)   |       | F1A  | G1A |
|        |     | 20110315: <Page 20> Change L27 from CS00004JA40 to CX121T30001<br><Page 20> Delete R208/ R251/ R433/ R475 for CS00003J951   |       | G1A  | A3A |
|        |     | 20110318: <Page 29> Change DC jack to DFPJ03MR043 (follow ZE6)  |       |      |     |
|        |     | 20110328: <Page 28> Change Thermal nut to MBZH5002012 (follow ZE6)  |       |      |     |
|        |     | 20110330: <Page 2> Change R236 PU connect from PM STPCPU# to PM STPCPU#_R   |       |      |     |
|        |     | 20110406: <Page 24> Change R329 from CS11202JB21(120ohm) to CS05102JB35(51ohm) PWR light<br><Page 24> Change R326/ R323/ R321 from CS12702JB14(270ohm) to CS12002FB25(200ohm) Blue light<br><Page 24> Change R327/ R324/ R322 from CS14702JB28(470ohm) to CS13302FB11(330ohm) Amber light<br><Page 22> Unstuff R341/ R330 for W/O LED RJ45 CONN (follow ZE6)<br><Page 27> Del T44 for no use of CIR uart function, will place T34 for ICT programming   |       |      |     |
|        |     | 20110407: <Page 28> Add GND PAD1 for LED ESD using<br><Page 16> Unstuff R100/ R142/ R143/ R132/ R96/ R97 for height limit   |       |      |     |
|        |     | 20110412: Change Q1/ Q27/ Q34/ Q35/ Q39/ Q42/ Q43 from BA0390400H0 to BA039040020 for EOL issue<br>Change PL1/ PL2/ PL6 from CX0R800R014 to CX12T800000 for EOL issue (EMI Sam provide)<br><Page 18> Change MRL from AL003661003 to AL002618001 for EOL issue (ZE6 2nd source)  |       |      |     |
|        |     | 20110413: <Page 30> Change PU3 from AL008206002 to AL008206000<br><Page 23> Add C388/ C389 stitching caps for monitor flickr issue<br><Page 11> Add net CPUSLP# / CPUSLP#_R and add R511/ R532 to reserve CPUSLP function   |       |      |     |
|        |     | 20110414: <Page 22> Change D35 from CY640P31Z08 to CY003100Z06 for cost down<br><Page 13> Stuff R451 to reserve thermal sensor function<br><Page 9> Unstuff C381/ C382/ R509/ R512/ R513/ R514/ U26 to reserve thermal sensor function<br><Page 27> Unstuff R175/ R160 to reserve thermal sensor function<br><Page4> Modify DDR DQ/ DQS/ DM signals to no swap type   |       |      |     |
|        |     | 20110418: <Page29-35> Change Power solution for ZE7 project<br><Page 23> Delete C389 for CRT DAC stitching cap<br><Page 30> Change JF1007 footprint to RC3720-SMT   |       |      |     |
|        |     | 20110420: <Page 11> Delete net CPUSLP# / CPUSLP#_R and delete R511/ R532 to remove CPUSLP function (nettop platforms only)<br><Page 20> Change R178/ R477 from 75ohm to 47ohm for earphone gain fine tune (follow ZE6)  |       |      |     |
|        |     | 20110422: <Page 18> Change MRL from AL002618001 to AL003661006(PT3661G-BB) for Lid switch issue<br><Page 30> Delete PC1032 for power request<br><Page 31> Delete PC1019; Add PR1104; Change PQ1001 (Dual MOS) to PQ1001 & PQ1008 (3X3 QFN)<br><Page 9> Un-stuff R149/ R151/ R478/ R479 to solve leakage issue<br><Page 18> Change C138 from 0.1U 6 to 4.7U 8 to solve hall sensor issue   |       |      |     |
|        |     | 20110425: <Page 25> Change U7 from AKE38FP0Z01 to AKE38FP0N01 for ICT MAC ID issue<br><Page 18> Change C138/ C318 from 4.7u 8 to 4.7u 6 (CH5471K9E07)   |       |      |     |
|        |     | 20110426: <Page 13> Add C389 0.1U 4 for TPT PWROK glitch issue<br><Page 2> Change Y2 from BG614318242 to BG614318F33 for new part   |       |      |     |
|        |     | 20110427: <Page 26> Change C267/ C268 from 22P/50V 4 to 10P/50V 4 for EMI request<br><Page 26> Add R511 and net MS_CLK_R for EMI request<br><Page 26> Change R271/ R285/ R290/ R299/ R305/ R313 from 0ohm to 33ohm for EMI request  |       |      |     |
|        |     | 20110428: <Page 26> Del R511 and net MS_CLK_R, change R303 from 0ohm to 33ohm for EMI request<br><Page 13> Reserve C390 30P 4 for EMI request<br><Page 20> Add C391 1n 4 for amic noise depressing (Realtek Vic suggest)<br><Page 31> Add PC1019/PC1032 2200p 4 for EMI request<br><Page 30> Change PC1043/ PC1046 from 330uF to 220uF; Change PL4 from 3.3uH to 2.2uH<br><Page 30> Change PR1098 from 4.7K ohm to 48.7K ohm  |       |      |     |
|        |     | 20110429: <Page 13> Stuff R85,R449,R455 for ZE7 A2 stage (Board ID PD)<br><Page 20> Change R178/ R477 from 47ohm to 56ohm to meet acer Full Scale Output Voltage (FSOV) spec<br><Page 13> Reserve R511 0ohm and RTCRST#_EC for RTC reset workaround solution<br><Page 19> Stuff CP1-CP6 for EMI Sam request   |       |      |     |
|        |     | 20110506: Rename<br><Page 17> Unstuff R138 to follow CRB  |       |      |     |
|        |     | 20110510: <Page 18> Change MRL from AL003661006(PT3661G-BB) to AL009132001 (CMOS type)<br><Page 18> Change C138 from 4.7U 6 to 1U 6; Unstuff R91 because MRL is CMOS type<br><Page 22> Change C4/C7 from 27P to 33P(CH03306JB04) by vendor fine tune result   |       |      |     |
|        |     | 20110516: <Page 11> Add R532/ R533 and net CPUSLP#_R / CPUSLP# (enable C6-state)<br><Page 17> Add R534/ R535 PU 2K for HDMI I2C to follow CRB<br><Page 24> Del SW4 for no use<br><Page 5> Change C334/ C335 from 18P 6 to 33P 4 for crystal vendor's report<br><Page 18> Add R536/ D44 for MRL EOS protection<br><Page 10> Modify USB0C pin<br><Page 13> Change CN5 to DPHS02FS032 for SMT issue<br><Page 13> Change R93/ R454/ R472/ R468 from CS03302JB29 to CS09092FB15 (RES CHIP 90.9 1/16W +-1%(0402)) to follow CRBv1.5<br>Remove Deeper Standby/ XDP/ DMIC/ USB charger function |       |      |     |
|        |     | 20110520: <Page 8> Change R99 from 12.1K to 121ohm to follow CRBv1.5<br><Page 8> Change R98 from 10K to 100ohm to follow CRBv1.5  |       |      |     |
|        |     | 20110525: <Page 30> Modify JP9 footprint to RC3720-SMT for SMT open issue   |       |      |     |
|        |     | 20110530: <Page 24> Modify LED4 from +3V to +5V Due to there is the internal series resistor in 3G/WLAN module, cause the forward voltage of LED4 is too small  |       |      |     |
|        |     | 20110531: <Page 29-35> Update power portion   |       |      |     |
|        |     | 20110601: <Page 26> Modify CN20 (Card reader CONN) footprint to 7in1-cm7r-052-h-d-44p-smt by SMT ME Peter request<br><Page 23> Change C140 from 0402 to 0603; Del C141<br><Page 29> Change PU9001 to PU2; Change PU2 footprint from QFN28-5X5-5-33P to QFN28-5X5-5-33P-SMT<br><Page 31> Add Power Jumper for power consumption measurement  |       |      |     |
|        |     |   |       |      |     |
|        |     |   |       |      |     |
|        |     |   |       |      |     |

| Model  | REV | CHANGE LIST  | MODEL | ZE7  |     |
|--------|-----|--|-------|------|-----|
|        |     |  |       | FROM | To  |
| ZE7 MB |     | 20110602: <Page 7> Del R490 and short for VCCCKDDR_VSM   |       | C1A  | D1A |
|        |     | 20110603: <Page 23> Del C215 for no use(DMIC stitching cap for RF)   |       | D1A  | E1A |
|        |     | 20110607: <Page 2> Delete R287/ R288/ T28 /T29 since SIO board was canceled  |       | E1A  | F1A |
|        |     | <Page 2> Delete R238/R239/ CLK_PCIE_MNC_XDP_N/ CLK_PCIE_MNC_XDP_P and short directly since XDP was canceled                                  |       | F1A  | G1A |
|        |     | <Page 25> Un-stuff R314,R294 since all of WLAN modules don't use SMBUS   |       | G1A  | A3A |
|        |     | <Page 21> Change USB CHARGE_ON to USB_EN#, delete R524/ USB_BC_EN and short , change U25 to AL000547005 since charge IC was canceled         |       | A3A  | B3B |
|        |     | <Page 31> Add PC123(100u/25V_6X5.8) to suppress VIN noise  |       |      |     |
|        |     | <Page 11> Stuff R105 1K for IOWME to follow CRB design   |       |      |     |
|        |     | <Page 13> Del R396/ R387, stuff R407/ R382 for PCH_GPIO12/ PCH_GPIO13 (PU for no use)  |       |      |     |
|        |     | <Page 4> Unstuff C200 /C190 for +0.75V_DDR_VTT   |       |      |     |
| B3B    |     | <Page 4> Unstuff C203 for +1.5VSUS   |       |      |     |
|        |     | <Page 7> Change R31/ R45/ R32 from 10uF_8 to 4.7uF_6   |       |      |     |
|        |     | <Page 7> Change C362 from 22uF_8 to 10uF_8   |       |      |     |
|        |     | 20110608: <Page 27> Reserve D22. stuff R281 for +3V_EC; Change D22 from BC000316Z07 to BCRB500VZ29   |       |      |     |
|        |     | <Page 31> Add PC123-PC127 to supress Vin noise   |       |      |     |
|        |     | <Page 27> Reserve D13/D14/ D17/D21 for HMPG  |       |      |     |
|        |     | 20110609: <Page 25> Un-stuff C9 since EM820W doesn't use Vpp   |       |      |     |
|        |     | <Page 13> Change Y4 from BG332768A01(20PPM/12.5PF) to BG332768542(20PPM/7PF), and change C348,C349 from 15pF_4 to 6pF_4                      |       |      |     |
|        |     | Change D8,D10,D19,D23,D24,D25,D39,D41 from BC000316Z07 to BCRB500VZ29  |       |      |     |
|        |     | 20110610: <Page 24> Change R330/ R327/ R325 to 51ohm_4 for Blue LED; Change R331 to 220ohm_4; Change R328 to 270ohm_4 for Orange LED         |       |      |     |
| Ramp   |     | --Gerber out for C-test--  |       |      |     |
|        |     | 20110614: <Page 6> Stuff R33 PU 1k ohm(CS21002JB34) to +3V for DBR# by Intel Nick confirming   |       |      |     |
|        |     | <Page 31> Change PR138 from CS41602FB00 to CS42742FB00 by Duncan request   |       |      |     |
|        |     | 20110622: <Page 24> Change R330 from CS05102JB35(51ohm) to CS03302JB29(33ohm) to meet LED brightness spec.                                   |       |      |     |
|        |     | <Page 24> Change R327 from CS05102JB35(51ohm) to CS03302JB29(33ohm) to meet LED brightness spec.   |       |      |     |
|        |     | <Page 24> Add R328 for CS12202FB14(220ohm) to meet LED brightness spec.  |       |      |     |
|        |     | <Page 24> Change R325 from CS05102JB35(51ohm) to CS11502FB1(150ohm) to meet LED brightness spec.   |       |      |     |
|        |     | <Page 24> Change R326 from CS13302FB11(330ohm) to CS14702JB28(470ohm) to meet LED brightness spec.   |       |      |     |
|        |     | 20110627: Change 0ohm resistors to short PAD   |       |      |     |
|        |     | 20110628: Remove common choke footprint  |       |      |     |
|        |     | Remove power short jumper  |       |      |     |
|        |     | <Page 2> Unstuff R229 CS00002JB38 for CPU_STOP# to follow checklist rev1.5   |       |      |     |
|        |     | <Page 5> Remove R411 / R412 CS00002JB38 and short for CRT_HSYNC / CRT_VSYNC  |       |      |     |
|        |     | <Page 13> Stuff R513 CS00002JB38 (0/J_4) for RTCSR#_EC ; Stuff R417 for PLT_RST#   |       |      |     |
|        |     | <Page 18> Stuff R26 CS00003J951 (0/J_6) for +5V_LCD (IVO panel)  |       |      |     |
|        |     | <Page 20> Stuff R203/R444 CS00003J951 (0/J_6) for audio ESD solution   |       |      |     |
|        |     | 20110630: <Page 20> Change CN15/CN13(Audio Jack CONN) footprint from phjk-2sj2326-002111-6p to phjk-2sj2326-002111-6p-smt for SMT open issue |       |      |     |
|        |     | Change PR65/PR66/PR39/PR29/PR153/PR22/PR36/PR152/PR160/PR161 footprint from RC0402 to short0402 by power Duncan request                      |       |      |     |
|        |     | <Page 31> Stuff PC7 CH14706KB18 (470p_4) for GFX issue   |       |      |     |
|        |     | <Page 10> Un-stuff C346/ C347 for no support PCI-E in 3G card  |       |      |     |
|        |     | <Page 18> Remove C324 for LCDVCC power   |       |      |     |
|        |     | <Page 20> Change C230,C221,C234,C247,C263,C265 from CH6101M9905 (10uF_6) to CH5471M9907 (4.7uF_6) for Audio power                            |       |      |     |
|        |     | <Page 5> Un-stuff R62 to reserve eDP function  |       |      |     |
|        |     | Unstuff C69; Change C20/CL37/CL57/C298/C310/C309/C387 from (10uF_8) to CH5472K9A02 (4.7uF_8)   |       |      |     |
|        |     | <Page 5> Change R38/R39 from 4.7K to 2.2K for EDID(follow CRB).  |       |      |     |
|        |     | <Page 29> Unstuff FUI (battery connector ESD solution)   |       |      |     |
|        |     | 20110705: <Page 25> Swap USBP7+/USBP7- to correct Wimax function.  |       |      |     |
|        |     | <Page 20> Stuff BC040201Z00 (TVS/6pF_4) at D9 for analog mic ESD solution  |       |      |     |
|        |     | 20110707: <Page 8> Stuff CS41002JB20(100K_4) at R474 for DDR3_DRAMRST#_R by Intel Nick confirming  |       |      |     |
|        |     | by Richtek's feedback  |       |      |     |
|        |     | 20110708: <Page 31> Change PC7 from CH14706KB18(470p/50V_4) to CH13306JB14(330p/50V_4) for GFX compensation.                                 |       |      |     |
|        |     | 20110711: <Page 18> Change R536 from CS00003J951(0_6) to CS04703F912(47_6) to increase hall IC ESD protection level                          |       |      |     |
|        |     | 20110719: <Page 20> Change R172/R497 from CS05602JB17(56_4) to CS04702FB16(47_4) for FAE Vic suggestion to meet acer FSOV spec               |       |      |     |
|        |     | 20110721: <Page 21> Change U23/U25 footprint from MSOP8-4_9-65-9p to MSOP8-4_9-65 to cancel GND pad for SMT open issue                       |       |      |     |
|        |     | 20110725: <Page 8> Add CH4103K1B08(0.1U/16V_4) cap footprint at C159 for Elpida DDR 2A issue debugging (to suppress glitch)                  |       |      |     |
|        |     | 20110727: <Page 8> Reserve 1U/10V_6 cap footprint at C388 for DDRAM_PWROK RC delay   |       |      |     |
|        |     | <Page 32> Un-stuff PR121 CS41002FB28(100K/F_4) PU for DDRAM_PWROK because D14 is un-stuff at EC side   |       |      |     |
|        |     | <Page 32> Del netname HMPG 1.5V and change to DDRAM_PWROK  |       |      |     |
|        |     | 20110804: <Page 20> Change L25 from CX12130001 (120ohm based) to CS00004JA40 (0_8) by EMI confirmed  |       |      |     |
|        |     | <Page19> Un-stuff CA122084N98 at CP1 - CP6 by EMI confirmed  |       |      |     |
|        |     | <Page26> Reserve C282/C284/C291/C296/C392/C393 CH01006JB08 (10p_4) by EMI confirmed  |       |      |     |
|        |     | 20110805: <Page 20> Reserve R520 0_6 footprint for analog mic ESD protection   |       |      |     |
|        |     | <Page 20> Stuff R501 0_6 for analog mic ESD protection   |       |      |     |
|        |     | 20110811: Change PC7 from 330p_4 (CH13306JB14) to 100p_4 (CH11006JB00) for power GFX issue   |       |      |     |
|        |     | 20110819: <Page 18> Change R75/R76 from CS01802JB13(18/J_4) to CS04702FB16(47/F_4)   |       |      |     |
|        |     | <Page 18> Change L16/L17 from CX8BA220007(0.5A/22ohm_6) to CS00003J951(0/J_6)  |       |      |     |
|        |     | 20110830: <Page 8> Change R537/R539 from CS00002JB38(0_4) resistors back to 0402 short pad for Elpida DDR 2A issue debugging                 |       |      |     |
|        |     | 20110831: <Page 26> Connect CN20(Card reader CONN) pin27 to GND by EMI Sam suggestion  |       |      |     |
|        |     | <Page 20> Add R520 CS00003J951(0_6) for analog mic ESD protection  |       |      |     |
|        |     | <Page 28> Modify Hole1 footprint from hg-c276do94x106p2 to ZE7-P3 for power button ESD solution  |       |      |     |
|        |     | <Page 28> Modify Hole15 footprint from HG-C276D98P2 to ZE7-P1 for touch pad ESD solution   |       |      |     |
|        |     | <Page 28> Modify Hole16 footprint from HG-C276D98P2 to ZE7-P2 for touch pad ESD solution   |       |      |     |
|        |     | <Page 28> Add GND PAD2 for touch pad ESD solution  |       |      |     |
|        |     |  |       |      |     |
|        |     |  |       |      |     |
|        |     |  |       |      |     |
|        |     |  |       |      |     |
|        |     |  |       |      |     |
|        |     |  |       |      |     |
|        |     |  |       |      |     |

|         |                 |     |              |  |           |  |
|---------|-----------------|-----|--------------|--|-----------|--|
| DOC NO. | PROJECT MODEL : | ZE7 | APPROVED BY: |  | DATE:     |  |
|         | PART NUMBER :   |     | DRAWING BY:  |  | REVISION: |  |



**Quanta Computer Inc.**  
**PROJECT : ZE7**

Size

Document Number

Rev

CAC

Change List3

Date: Wednesday, August 31, 2011

Sheet 42 of 42